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A 90 dB, 85 MHz operational transconductance amplifier (OTA) using gain boosting technique

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A 90 dB, 85 MHz

Operational Transconductance Amplifier (OTA)

Using Gain Boosting Technique

by

Ashish C Vora

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ABSTRACT

Gain and speed are the two most important parameters of an amplifer. Optimizing an amplifier for both of these parameters leads to contradicting demands. Various architectures have been reported to obtain high gain from the circuits. Cascode circuits are widely used in circuit design at places where high gain and high output impedances are required. Different architectures like triple cascode topology, dynamic biasing and a positive feedback amplifier have been used to obtain high gains. These architectures have been compared in this thesis along with drawbacks and advantages of each.

This thesis describes a regulated cascode circuit (RGC) which provides a high output resistance which, in turn, leads to high gain as compared to a normal cascode circuit (optimally biased cascode – OBC). A complete analysis of the circuit is presented in this thesis which shows how this circuit leads to a high gain and resistance at output. A brief comparison between the regulated cascode and an optimally biased cascode (normal cascode) is also described. This thesis provides a considerable insight into the overall operation and advantages of the regulated cascode circuit. Later in this thesis a design of a high gain amplifier using this regulated cascode configuration is presented. This design overcomes various limitations and drawbacks of the various previously described architectures.

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INTRODUCTION

1. 1 INTRODUCTION

The operational amplifier (op-amp) is one of the most versatile and important building blocks in analog circuit design. Op-amps that are designed to provide transconductance should provide very high output impedance and hence provide very good isolation. The output voltage, current, output impedance and the gain of the op-amp can be set in order to suit the application. These qualities of op-amp are utilized in circuits like integrators, differentiators, buffers, analog-to-digital converters and digital-to-analog converters.

The amplifier's performance is usually limited due to various factors such as gain, bandwidth, slew rate, voltage swing, etc. Gain and speed are the two important parameters of the operational amplifier. Due to shrinking of power supplies the dynamic range of the overall circuit is also reduced, due to which the

signal handling capability of the circuit is also limited. Without a thorough understanding of the operation and the various parameters of the operational amplifier, the circuit designer cannot determine the overall response of the system. Op-amps have a wide range of applications owing to their performance as mentioned before.

This thesis presents a 90 dB, 85 MHz gain bandwidth telescopic cascode amplifer using the gain boosting technique. Initially this work describes a regulated cascode circuit (RGC) which provides a high output resistance which leads to high gain as compared to a normal cascode circuit (optimally biased cascode – OBC). A complete analysis of the circuit is presented in this thesis which shows how this circuit leads to a high gain and resistance at output. A brief comparison between the regulated cascode and an optimally biased cascode (normal cascode) is also described. This thesis provides a considerable insight into the overall operation and advantages of the regulated cascode circuit. Later the design of a high gain amplifier using this regulated cascode configuration is presented[1]. This design overcomes various limitations and drawbacks of the various previously presented described architectures.

[1] A complete list of specifications is mentioned in Chapter 4, Section 4.1 on page 49.

1. 2 ORGANIZATION OF THESIS

This thesis is organized into five chapters. In Chapter 2, various commonly used amplifier configurations are presented. Then a literature review covering various operational amplifier configurations previously used to obtain high gain and speed is presented. Some basic advantages and disadvantages of each configuration are shown. Also a brief description of the various characteristics of an ideal operational amplifier is mentioned.

In Chapter 3, a complete analysis of the gain boosted cascode (regulated cascode) circuit is presented. This includes a complete description and working of the circuit. It is also shown how the gain of the circuit increases without affecting other parameters. Also, a complete stability (pole-zero) analysis is presented in relation to the design of certain critical components of the circuit. Low-frequency and high-frequency performance is also analyzed along with the settling time behavior of the circuit.

In Chapter 4, a telescopic cascode amplifier with gain boosting is designed using the gain boosted cascode configuration. An amplifier with a gain of 90 dB and 85 MHz unity gain frequency is designed. This is presented as a proof of concept for the gain boosted cascode circuits.

Finally, in Chapter 5, a summary and conclusions of this work are presented. Some suggestions regarding the future work that can be pursued are also presented.

Chapter 2

BACKGROUND OF OPERATIONAL AMPLIFIERS

Five commonly used operational amplifiers architectures are briefly presented here. Advantages and limitations of these architectures are also summarized and some solutions suggested in the literature to overcome these limitations are also presented. All these commonly used amplifiers shown in this chapter are fully differential, and might need common mode feedback circuits in practical applications. The performances of all of these different commonly used configurations are summed up in Table 2.1.

A brief literature review describing previously done work related to high gain operational amplifier architectures and mechanisms is described in this chapter. Various methods used for increasing the gain of the amplifier used in the

literature are presented along with the drawbacks of each method. A brief summary of results from this review is also presented which leads to the motivation for this particular work.

Later in the chapter a brief description of various operational amplifier parameters that determine the quality and usefulness of the amplifiers is also provided as a guide.

The difference between an Operational Transconductance Amplifier (OTA) and an Operational Amplifier (op-amp) is that the op-amp has got an output buffer so that it is able to drive resistive loads. An OTA can only drive capacitive loads.

2. 1 DIFFERENT OP-AMP CONFIGURATIONS

Five commonly used basic operational amplifier architectures are mentioned here. These are basic topologies presented here and various modifications have been implemented in these topologies to obtain the desired performance [1], [2], [3], [4], [5], [6].

a) Single-Stage OTA

This configuration is shown in Figure 2.1. This is the least complex OTA, and hence its speed can be very high.

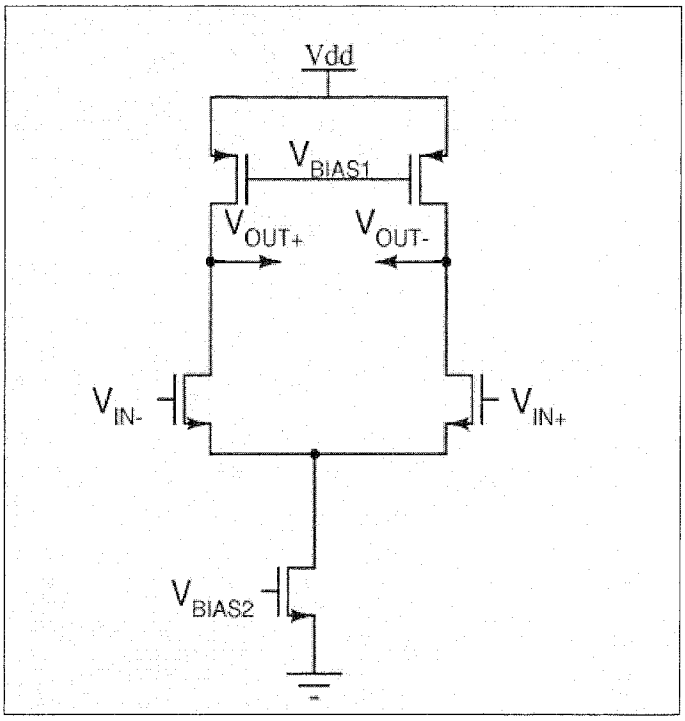


Figure 2.1: Single-stage OTA

The drawback is that the gain is rather low due to the fact that the output impedance of this configuration is relatively low ($r_o \cong O(10^1 - 10^2 k\Omega)$). This low impedance also leads to high unity gain bandwidth and hence high speeds.

b) Two-Stage OTA

By adding another stage we get a two-stage amplifier. This is shown in Figure 2.2. This modification increases the gain up to a certain extent as compared to a single stage OTA. But this addition of an extra stage also increases the complexity. The increased complexity will reduce the speed in comparison to a single stage amplifier.

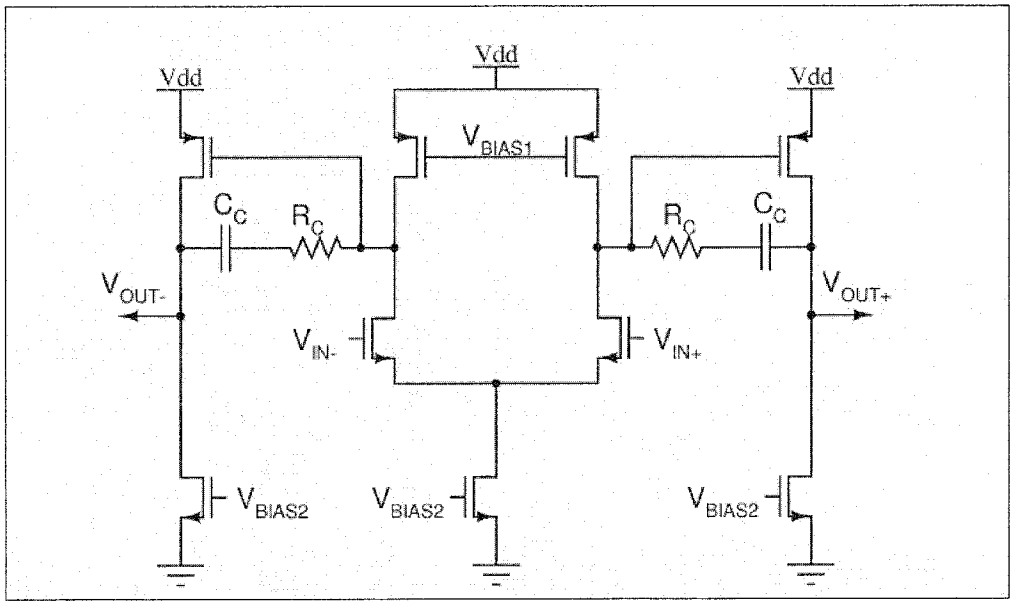


Figure 2.2: Two-stage OTA

This configuration needs a suitable compensation scheme to stabilize the amplifier. One of the various compensation circuits (R_C, C_C) is also shown in Figure 2.2.

c) Telescopic Cascode OTA

This configuration is shown in Figure 2.3. The reason why the gain of the single-stage OTA is low is that it has low output impedance. One way of increasing the impedance is to add some transistors at the output including using an active load. Transistors are stacked on top of each other. The transistors are called "cascodes", and will increase the output impedance and thereby increase the gain.

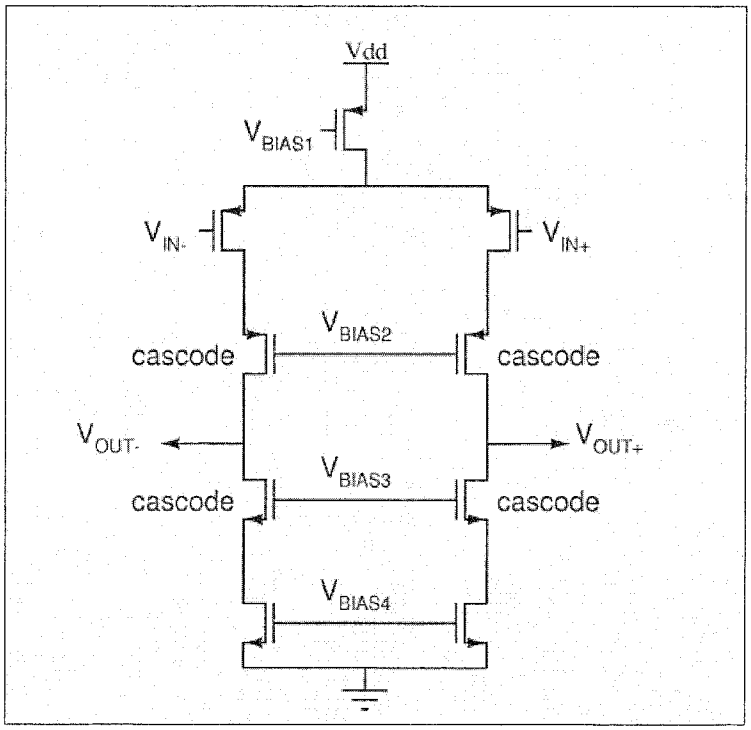


Figure 2.3: Telescopic Cascode OTA

The telescopic cascode has got high gain as well as high speed, but by adding more transistors the voltage swing at the output is reduced. This is not desirable in systems with low supply voltages. Techniques to increase the voltage swing have been reported in the literature, [7].

d) Regulated Cascode (Gain Boosting) OTA

This configuration is shown in Figure 2.4. Regulated cascode (or gain boosting) can be used to even further increase the gain without decreasing output voltage swing.

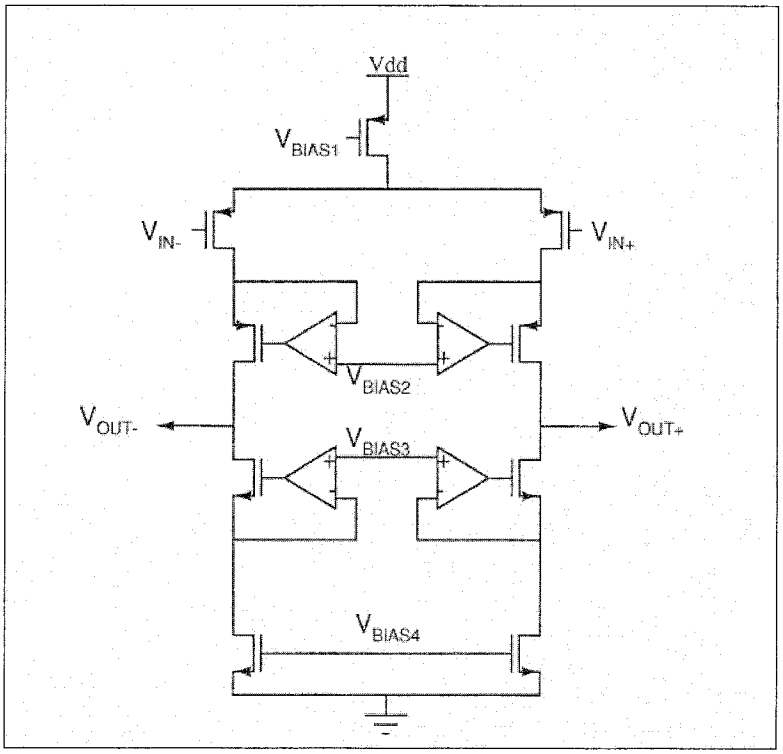


Figure 2.4: Regulated cascode (gain boost) OTA

This gain boosting technique has been reported by Eduard Sackinger and Walter Guggenbuhl [8]. By applying this method the gain is increased by approximately the gain of the gain boost amplifiers[2].

The drawback of this configuration is that these extra amplifiers might reduce the speed of the overall amplifier. Hence, they should be designed to have a large bandwidth so as not to affect the bandwidth of the entire configuration.

e) Folded Cascode OTA

This configuration is shown in Figure 2.5. The folded cascode amplifier is in a way a compromise between the two-stage amplifier and the telescopic cascode amplifier. It permits low supply voltage, still having a rather high output voltage swing and the input and output common mode levels can be designed to be equal. Its gain is lower than for the two-stage amplifer and its speed is lower than for the telescopic cascode, which makes it a good compromise between these two amplifiers.

Various techniques have been reported to improve the gain and bandwidth of this configuration [9].

[2] For a complete mathematical analysis and derivation refer Chapter 3, Section 3.3.b on page 37.

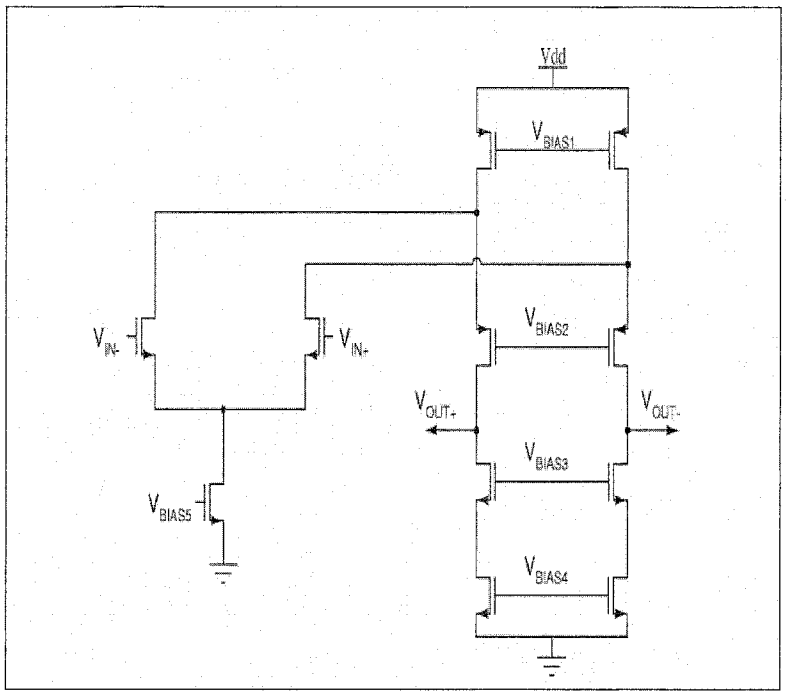


Figure 2.5: Folded cascode OTA

2. 2 LITERATURE REVIEW

Speed and accuracy are two of the most important parameters of any analog circuits. It is difficult to optimize any circuit for both these parameters and a compromise is to be reached between the two. Optimizing the circuit for both leads to contradictory demands. In many analog circuits like switched-capacitor filters [1], [10], [11], algorithmic A/D converters [12], sample and hold amplifiers [13] and pipelined A/D converters [14], speed and accuracy are determined by the settling behavior of the operational amplifiers. Fast settling requires high unity gain frequency of the amplifier and accurate settling requires high gain of the amplifier.

Designing a CMOS operational amplifier that provides both high gain and high unity gain frequency has always been a challenging problem. High gain requirement leads to multistage designs, designs involving long channel devices biased at low currents, whereas high unity gain frequency requirement leads to single stage design with short channel devices biased at high currents.

It is possible to obtain high unity gain frequencies with current submicron processes but at the same time the intrinsic gain of the transistor goes down [15], making it more difficult to attain high gain from the amplifier. Hence various new circuit topologies have been implemented to solve this problem.

Cascoding the transistors is a well-known solution to enhance the DC gain of the amplifier without degrading its frequency response. But the amount of increase in DC gain obtained by cascoding is not sufficient in many cases [1], [2], [3].

Dynamic biasing of transistors was another approach shown to provide high gain as well as high settling speeds [4], [5], [6]. In this approach bias currents are decreased as a function of time or as a function of amplitude. However, this approach reduces the unity gain frequency which makes the later part of settling very slow.

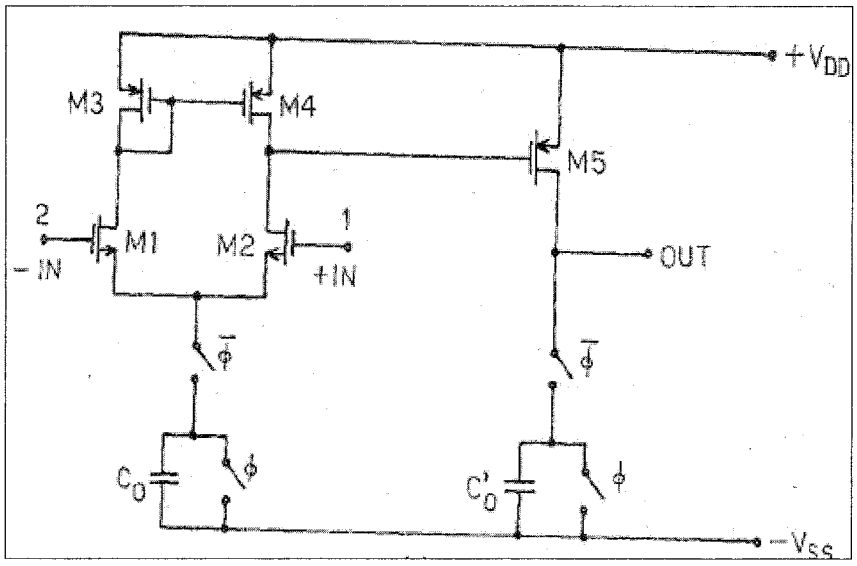


Figure 2.6: Dynamically biased CMOS amplifier [5]

A dynamic amplifier regulates its own bias current based upon the signal levels. The amplifier starts its operation with large bias current which means that

the amplifier is fast. Then the current decreases so that the gain increases towards its maximum.

A triple cascode amplifier has been reported in [16]. This approach has two major disadvantages. First, every transistor added in the signal path adds an extra pole in the system. Hence in order to compensate for these poles and to obtain sufficient phase margin minimum load capacitance required has to be increased. This increase in load capacitance results in lower unity-gain frequency. Secondly, each stacked transistor reduces the output swing of the design.

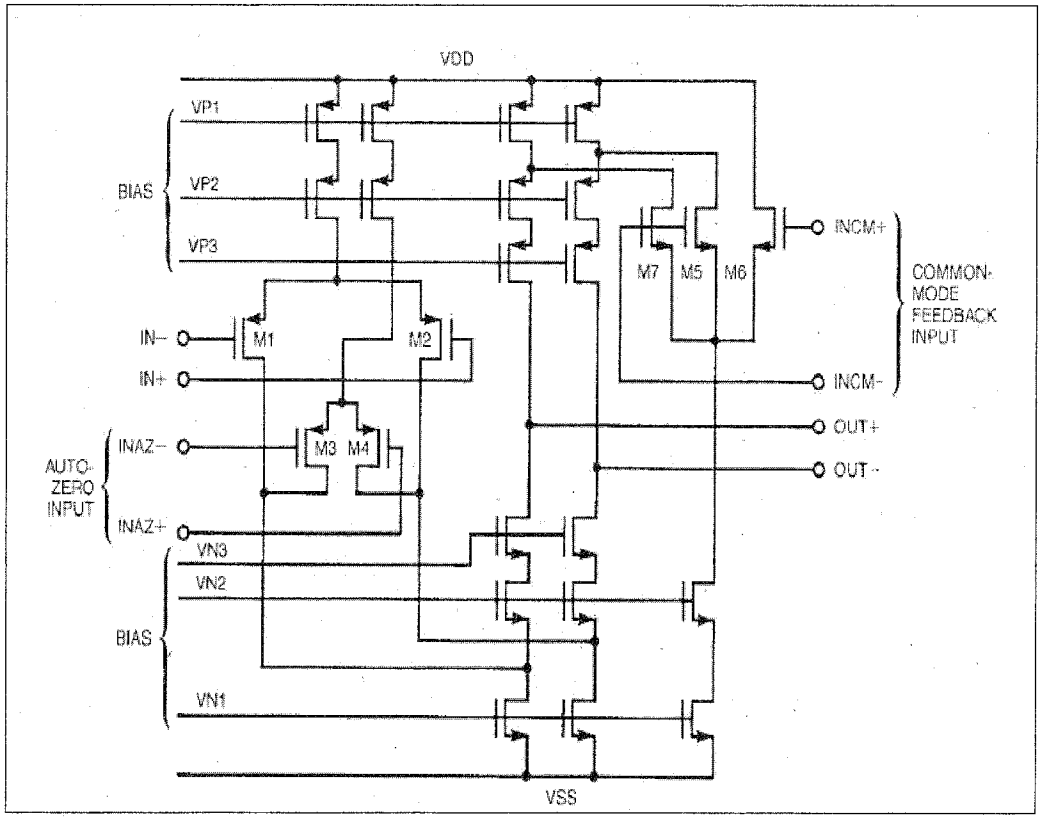


Figure 2.7: Triple cascode amplifier schematic [16]

This amplifier has a folded cascode input differential stage followed by a triple cascoded output stage. Triple cascoded transistors at the output give very high gain from this configuration but at the same time stacking three transistors reduces the available swing at the output.

Positive feedback is used to enhance the gain of the amplifier in [2]. However this approach is limited by matching. Also a significant gain enhancement is not obtained using this approach.

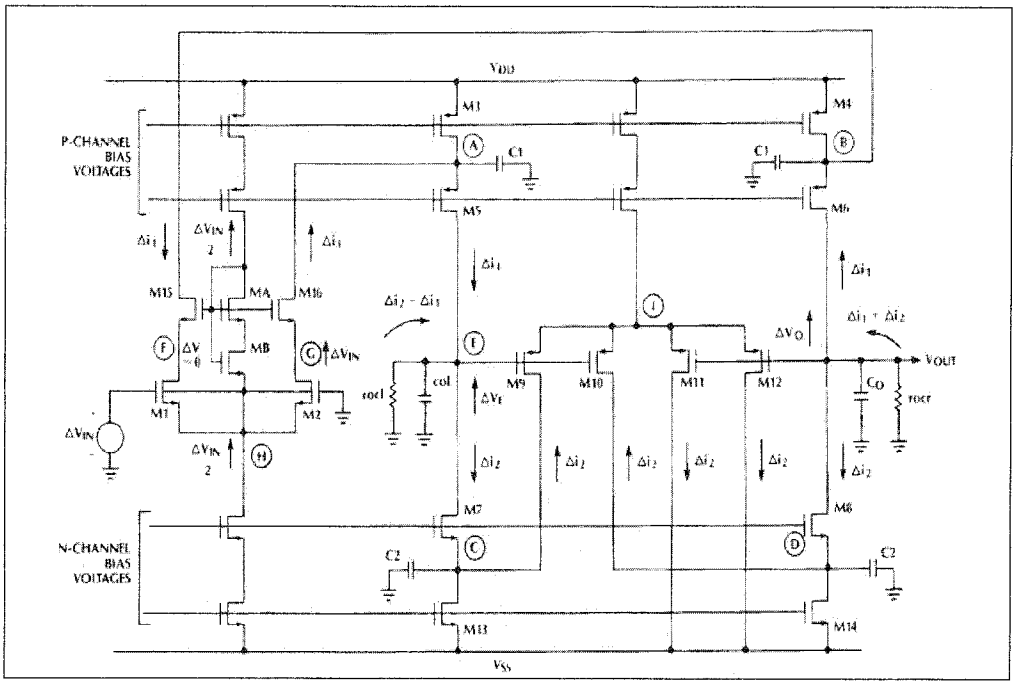


Figure 2.8: Gain enhancement using positive feedback [2]

For high-Q, high frequency switched capacitor filters the amount of gain obtained by this approach is not significant. Even a moderate Q of 25 and a deviation of 1 percent requires a op-amp gain of 75 dB [1], [2].

Some of the designs from the literature are summarized below:

1: Triple Cascode topology, 85 dB gain, $\pm$ 5 V supply, $\pm$ 3.5 V swing, 5 um technology [12]

2: Positive feedback topology, 70 dB gain, 25 MHz unity gain bandwidth, 18 V/us slew rate, 10 mW power, 3 um technology [2]

3: Dynamic Amplifier topology, 65 dB gain, $\pm$ 5 V supply, 0.25 V/us slew rate, 5 um technology [6]

Hence we aim at a DC gain of at least 85 dB combined with unity gain frequency of at least 70 MHz.

In [17] a regulated cascode stage has been presented that increases the gain of a normal cascode stage without affecting the frequency behavior to a large extent.

This work describes this regulated cascode technique in detail. A complete analysis and working of this technique is presented. A complete stability analysis, high frequency behavior and settling behavior are described. Next, a circuit implementation of this technique in which a telescopic cascode circuit is designed using gain boosting topology, is presented as a proof of concept for this topology. This technique has been used in this thesis to design an operational amplifier with a gain greater than 85 dB and a unity gain bandwidth greater than 80 MHz.

2. 3 COMPARISON OF DIFFERENT CONFIGURATIONS

The table presents a comparison of basic op-amp parameters for different configurations described above.

TABLE 2.1: Comparison of various op-amp parameters for different op-amp configurations

	Gain	Output Swing	Speed	Power	Noise
Telescopic Cascode	Medium	Medium	Highest	Low	Low
Folded cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Regulated Cascode	High	Medium	Medium	Highest	Medium

2. 4 OP-AMP TERMINOLOGY

There are many parameters which determine the quality of the operational amplifier. Here is a brief explanation of commonly considered parameters.

1. **Input offset voltage**: An ideal operational amplifier will give an output of 0 V if both of its inputs are shorted together. A real op amp will have a non-zero voltage output even if its inputs are shorted together. This is the effect of its input offset voltage, which is the slight voltage present across its inputs brought about by its non-zero input offset current. In essence, the input voltage offset is also the voltage that needs to be applied across the inputs of an op amp to make its output zero.

2. **Open loop gain**: This is the ratio of the op amp's output voltage to its differential input voltage without any external feedback.

3. **Common Mode Rejection**: This is the ability of an operational amplifier to cancel out or reject any signals that are common to both inputs, and amplify any signals that are differential between them. Common mode rejection is the logarithmic expression of CMRR.

$$CMR=20\log CMRR.$$

CMRR is simply the magnitude of the ratio of the differential gain to the common-mode gain.

4. **Gain-Bandwidth product**: For single pole amplifiers this is the product of the op amp's open-loop voltage gain and the frequency at which it was measured.

5. **Slew Rate**: This is the maximum rate of change of the op amp's output voltage when the input signals are large.

6. **Settling Time**: This is the length of time for the output voltage of an operational amplifier to approach, and remain within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step.

7. **Phase Margin**: An op amp will tend to oscillate at a frequency wherein the loop phase shift exceeds -180°, if this frequency is below the closed-loop bandwidth. The closed-loop bandwidth of a voltage-feedback op amp circuit is equal to the op amp's bandwidth at unity gain, divided by the circuit's closed loop gain.

   The phase margin of an op amp circuit is the amount of additional phase shift at the closed loop bandwidth required to make the circuit unstable

(i.e., phase shift + phase margin = -180°). As phase margin approaches zero, the loop phase shift approaches -180° and the op amp circuit approaches instability.

Typically, values of phase margin much less than 45° can cause problems such as "peaking" in frequency response, and overshoot or "ringing" in step response. In order to maintain conservative phase margin, the pole generated by capacitive loading should be at least a decade above the circuit's closed loop bandwidth.

8. **Output voltage swing**: This is the maximum output voltage that the op amp can deliver without saturation or clipping for a given load and operating supply voltage.

9. **Input Common Mode Range (ICMR):** This is the maximum voltage (negative or positive) that can be applied at both inputs of an operational amplifier at the same time, with respect to the ground.

10. **Total Power dissipation:** The total DC power supplied to the op amp minus the power delivered by the op amp to its load.

11. **Power Supply Rejection Ratio**: PSRR is a measure of an op amp's ability to prevent its output from being affected by noise or ripples at the power supply. It is computed as the ratio of the change in the op amp's output voltage to the change in the power supply voltage (caused by the power supply change). It is often expressed in dB.

12. **Input Bias Current:** The average of the currents into the two input terminals with the output at zero volts.

13. **Input Offset Current:** The difference between the currents into the two input terminals with the output held at zero.

14. **Differential Input Impedance:** The resistance between the inverting and the non-inverting inputs. This value is typically very high.

15. **Common-mode Input Impedance:** The impedance between the ground and the input terminals, with the input terminals tied together. This is a large value, of the order of several tens of megohms or more.

16. **Output Impedance**: The output resistance is typically less than 100 Ohms.

17. **Average Temperature Coefficient of Input Offset Current**: The ratio of the change in input offset current to the change in free-air or ambient temperature. This is an average value for the specified range.

18. **Output offset voltage**: The output offset voltage is the voltage at the output terminal with respect to ground when both the input terminals are grounded.

19. **Output Short-Circuit Current:** The current that flows in the output terminal when the output load resistance external to the amplifier is zero ohms (a short to the common terminal).

20. **Channel Separation:** This parameter is used on multiple op-amp ICs (device in which two or more op-amps sharing the same package with common supply terminals). The separation specification describes part of the isolation between the op-amps inside the same package. It is measured in dB. The 747 dual op-amp, for example, offers 120 dB of channel separation. From this specification, we may state that a 1 μV change will occur in the output of one of the amplifiers, when the other amplifier output changes by 1 volt.

Chapter 3

GAIN BOOSTING THEORY

3. 1 INTRODUCTION TO GAIN BOOSTING

For VLSI and high-frequency circuits, transistors with minimum feature size are often used. Such transistors exhibit pronounced channel-length modulation and carrier multiplication due to hot carrier effects, even at relatively low voltages, as well as a moderate transconductance. The maximum dc-voltage gain achievable with these transistors is therefore restricted to relatively small values. Scaling devices down, according to most scaling laws, further reduces this gain.

As CMOS design scales into low-power low-voltage regime, designing analog functional blocks under limited supply voltage becomes more and more difficult. One typical example is the basic gain stage. Cascoding is the mostly used technique to achieve high gain compared to two-stage designs because of its superior frequency response. However, we quickly run into headroom problems while trying to cascode more transistors in a stack under limited supply voltage. A gain-boosting technique was introduced to remedy this problem. It allows increasing the DC gain of the operational amplifier (op amp) without sacrificing the output swing of a regular cascode structure. The main idea behind gain boosting is to further increase the output impedance without adding more cascode devices. Furthermore, it has been pointed out that the gain-boosting technique decouples the gain and the frequency response of the amplifier. In such cases the regulated cascode circuit with minimum-size transistors can be applied to obtain a small circuit area, good frequency response, and high gain simultaneously. It is therefore possible to achieve high speed and high gain at the same time. These features are especially desirable in high-speed, high-dynamic range applications like switched-capacitor filters, track and hold circuits, and A/D converters.

3. 2 NORMAL CASCODE CIRCUIT

A cascode is a two transistor stack used to obtain high gain and high output impedances. A cascode consists of a common source configuration followed by a common gate stage. This cascode configuration has two basic advantages over the normal configuration. The first is that it provides high output impedance which is useful in obtaining high gain from the circuits. The second is that it reduces the capacitances at input in comparison to the normal configuration which helps in obtaining high frequency response.

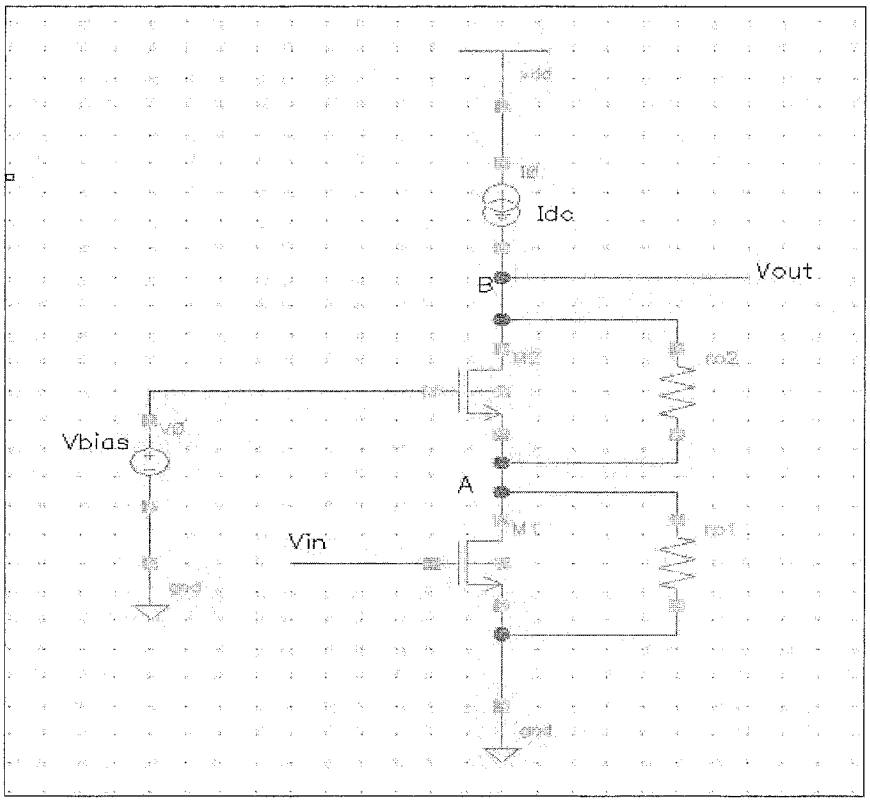


Figure 3.1: A typical cascode circuit biased by a current source.

1. Output impedance:

This is one of the advantages of the cascode circuit that is used in various applications. Consider in Figure 3.1 the action of the circuit in response to the test current i_x applied at node B. This will flow through r_{o2} and raise the voltage at intermediate node A. If there is no input given to M1 then $v_A = i_x r_{o1}$. However as v_A is driving M2 it will produce a transconductance current $i_{ds}(M2) = -g_{m2} v_A$. This will flow through r_{o2} in addition to the externally applied i_x. Thus

$$v_x = v_B = v_A + (i_x + g_{m2} v_A) r_{o2}$$

Hence the output impedance is

$r_{o1} + (1 + g_{m2} r_{o1}) r_{o2}$ which is usually taken as $g_{m2} r_{01} r_{02}$.

Hence $R_{out} = g_{m2} r_{01} r_{02}$.

The other important thing is that the input impedance at the intermediate node A is very small, usually taken to be $1/g_{m2}$. Thus the Miller effect on the capacitance C_{gd}(M1) is greatly reduced. This helps a great deal in designing circuits with good high-frequency response.

2. Gain:

The cascode configuration gives more gain as compared to a simple common source configuration. The gain is taken to be the product of the transconductance

and the output impedance. The gain depends on the loading of the amplifier. The load impedance should be suitably high or the effect of high output resistance of the cascode configuration is lost.

3. 3 REGULATED (Gain Boosted) CASCODE

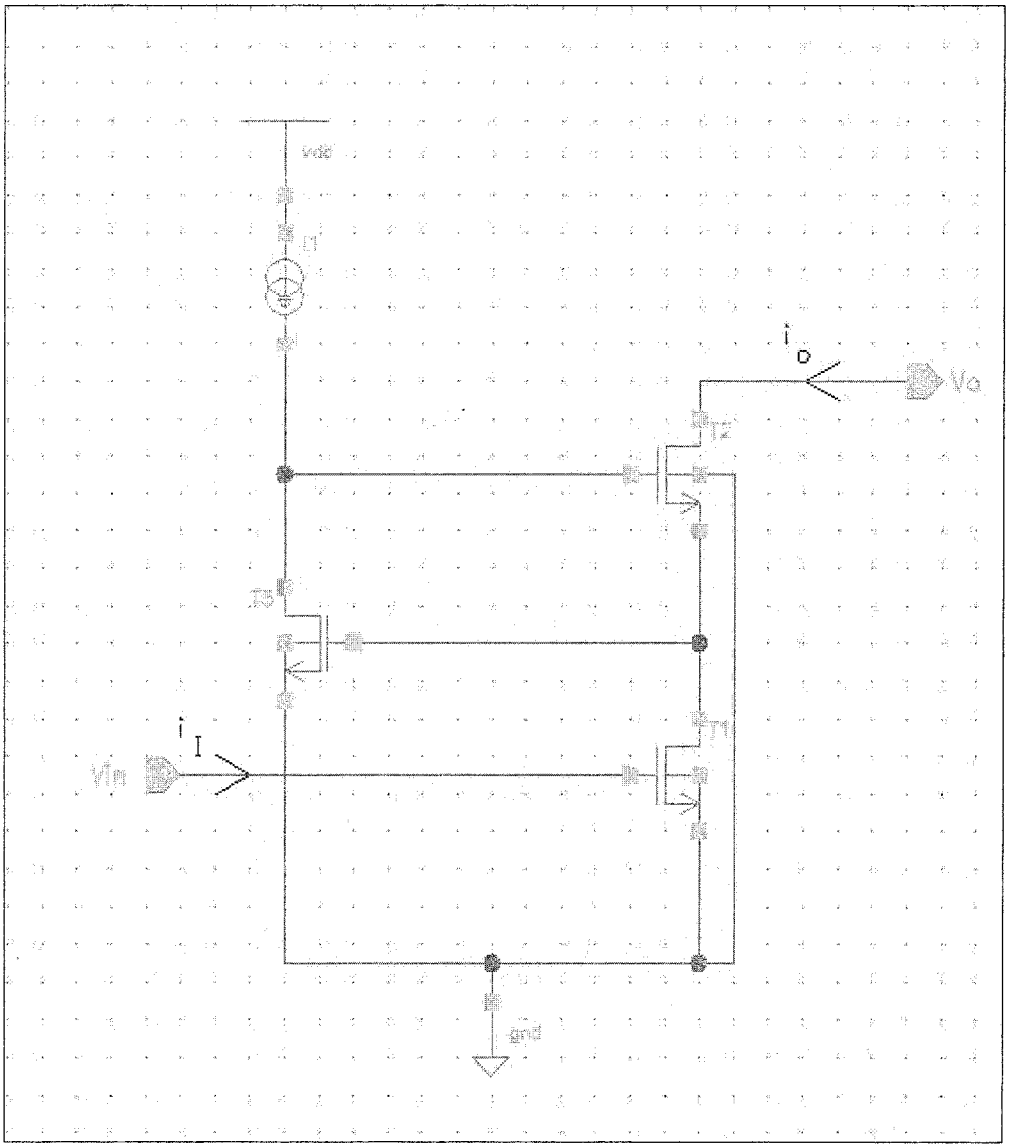


Figure 3.2: Regulated Cascode Circuit

The main advantage of this type of circuit is that the output impedance is more than the regular cascode and the output voltage range is also increased as compared to the normal cascode.

The operating principle is as follows: Transistor T_1 converts the input voltage v_I into drain current i_o that flows through the drain-source path of T_2 to the output terminal. The drain-source voltage must be kept stable so as to obtain high output resistance. In normal cascode this is done by loading the drain with the low source input resistance of T_2 but here there is a feedback loop consisting of an amplifier T_3 and I_1 and T_2 as a follower. Hence the drain-source voltage of T_1 is regulated to a fixed value.

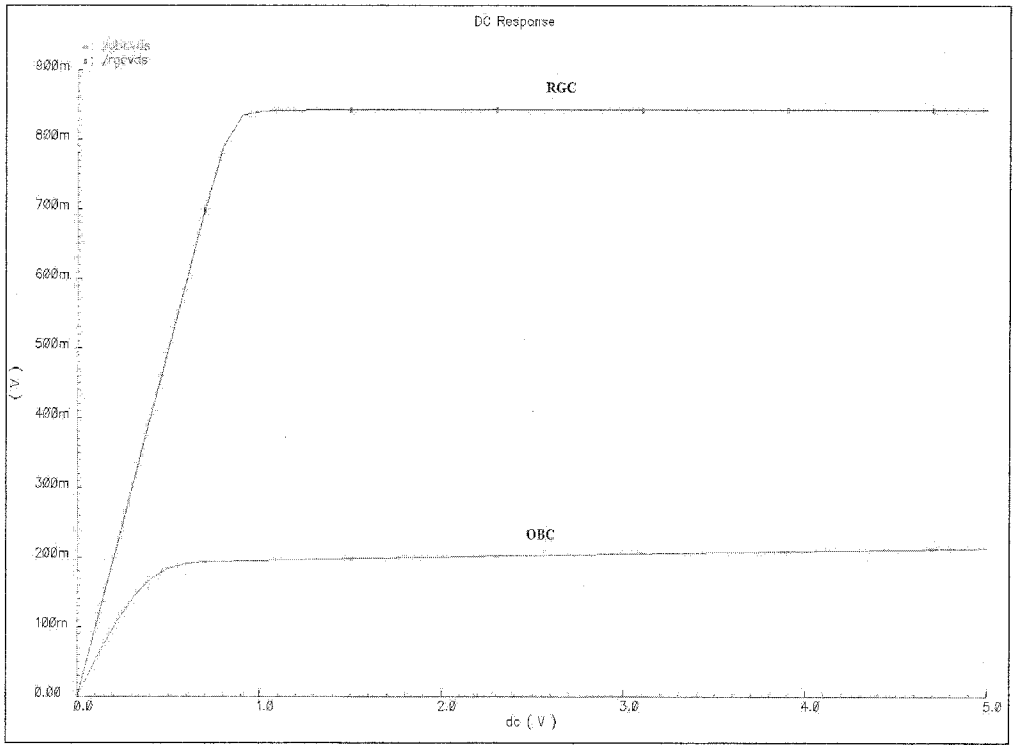


Figure 3.3: VDS variation for main input transistor for regulated cascode (RGC) and normal cascode (OBC) configurations

Figure 3.3 shows how the drain-source voltage of T_1 is regulated to a fixed value. The upper line shows V_{ds1} variation for regulated cascode configuration and the lower line shows the same for a normal cascode configuration. It is observed that this variation (i.e., upward slope) is higher in case of normal cascode circuit as compared to regulated cascode.

The output resistance of this circuit is $R_{out} \cong A_3 g_{m2} r_{01} r_{02}$, where A_3 is the gain of the feedback transistor T_3. Since the gain of the circuit is directly related to the output resistance the gain also increases by the same factor.

The other advantage of this configuration is that it is easy to control the drain-source voltage drop of the transistor T_1 as it is directly related to the gate-source voltage of T_3 which in turn depends on current I_1. Hence the transistors can be sized so as to obtain minimum drain-source voltage drop across T_1 for increased head room to stack more transistors while maintaining it in saturation mode. The other advantage of this configuration is that the feedback loop increases the stability of the circuit even when the transistor T_2 is in ohmic region, thereby increasing the usable range of the circuit.

3.3.a ANALYSIS and OPERATION

In Figure 3.2 let the input voltage v_I = V_{gs1} be a constant value. For the transistor T_1 to operate in saturation its drain voltage V_{ds1} must be such that $V_{ds1} \geq V_{gs1} - V_T$. Now to obtain a maximum possible output swing this voltage V_{ds1} must be as low as possible without taking the transistor T_1 out of saturation. As this voltage V_{ds1} is controlled by the feedback loop of T_3 and I_1, assuming that T_3 is operating in strong inversion we have the equation:

$$V_{ds1} = V_{gs1} - V_T = \sqrt{\frac{2I_1}{\beta_3}} + V_T \quad \text{where, } \beta_3 = \mu C_{ox} \frac{W_3}{L_3}$$

This gives us the condition that $V_{gs1} \geq 2V_T$. If T_3 can be operated in weak inversion then this condition doesn't apply. Using the drain current equations for weak inversion region we obtain the gate voltage required for optimal biasing of T_1. For the weak inversion region we get:

$$i_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS}}{\eta V_T}\right)$$

where I_{D0} is the subthreshold current typically in the orders of nA.

$$V_{ds1} = V_{gs1} - V_T = \eta V_T \ln\left(\frac{L_3 I_1}{W_3 I_{D0}}\right)$$

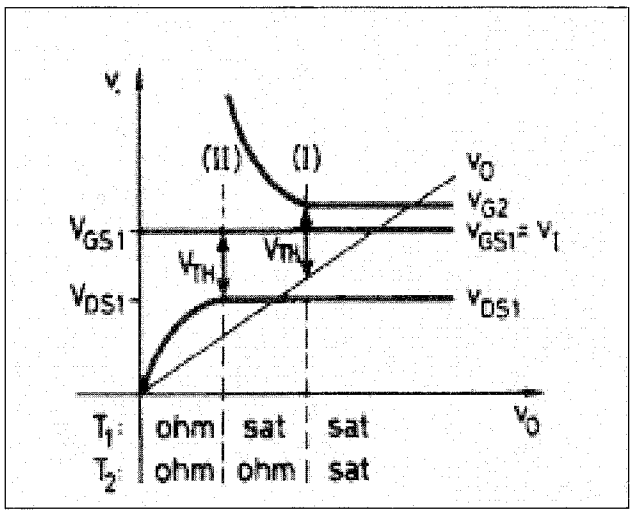


Figure 3.4: Transistor gate and drain voltages of the RGC as a function of output voltage [8].

Figure 3.4 shows the operation of the circuit with respect to the output voltage of the circuit. If the circuit is optimally biased so that $V_{ds1} = V_{gs1} - V_T$ then in order to conduct output current the gate bias to T_2 should be such that it is one threshold above the V_{ds1}. If the output voltage v_o is reduced starting from high values (power supply value) then as shown in Figure 3.4 transistor T_2 first leaves the saturation region and if this voltage is reduced further then the transistor T_1 goes out of saturation.

At point I as v_o drops below V_{g2} by one threshold value the transistor T_2 leaves saturation region and enters into the ohmic region. Hence more gate bias is required by T_2 to drive the current forced by T_1. The increase in gate voltage of T_2 is taken care of by the feedback loop.

Further, as the output voltage decreases more then point II is reached where even the increase in gate voltage of T_2 is not sufficient to drive the saturation current forced by T_1. Hence at this point even transistor T_1 leaves saturation and enter the ohmic region. During the whole operation of the circuit T_3 always remains in saturation as $V_{ds3} > V_{gs3}$.

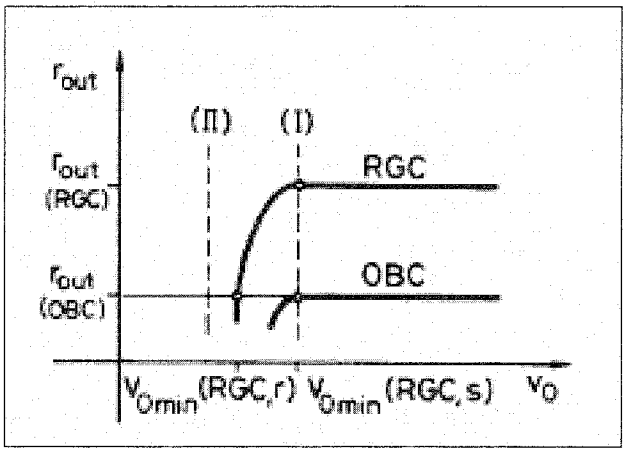
Table 3.1 below shows the region of operations of transistors as the output voltage is decreased starting from the maximum possible value.

POINT	**TRANSISTOR T_1**	**TRANSISTOR T2**
Before point I	Saturation	Saturation
I	Saturation	Ohmic
II	Ohmic	Ohmic

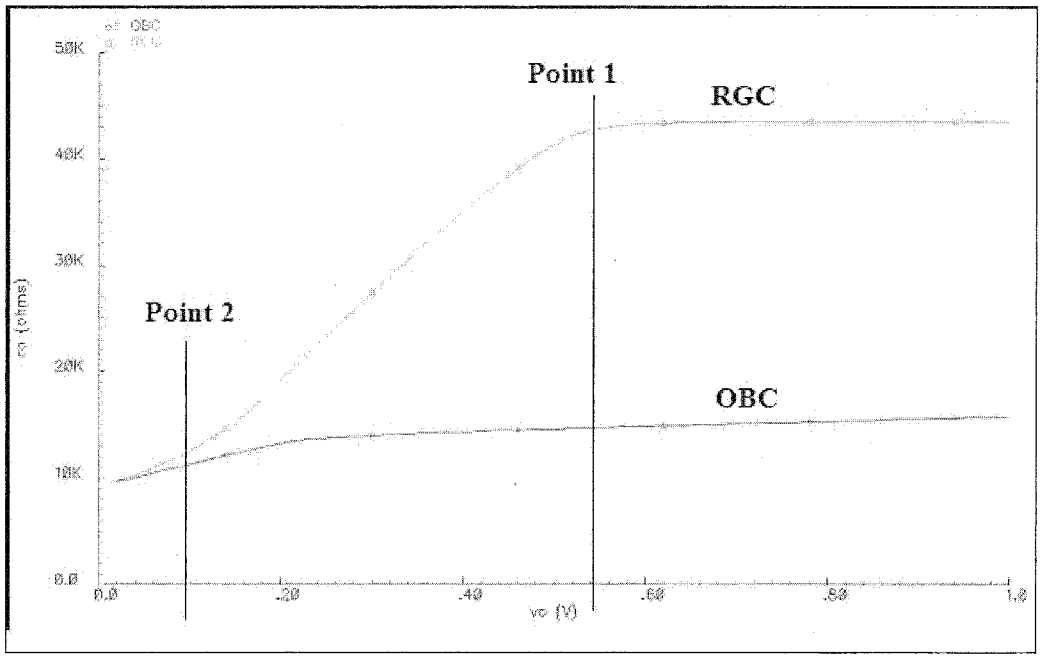
Table 3.1: Regions of operation of the transistors T_1 and T_2 as the output voltage is decreased starting from the maximum possible value.

The minimum allowed voltage at the output is thus the voltage required by transistors T_1 and T_2 to remain in saturation. The voltage across each transistor is $V_{gs} - V_T$. Thus the minimum output voltage is $V_{gs1} - V_T + V_{gs2} - V_T$. This voltage is

the same as that required in case of a normal cascode circuit to keep both transistors in saturation.



(a)



(b)

Figure 3.5: Output resistances of regulated cascode circuit (RGC) and optimally biased circuit (OBC) as a function of output voltage;

(a) conceptual behavior (b) simulated behavior

But in case of regulated cascode circuit the minimum output voltage is defined as the voltage at which the small signal output resistance of the regulated cascode is the same as the normal cascode in saturation.

Figure 3.5 shows the variation in the output resistance of both the cascode configurations From this it is clear that the output voltage at which the resistance of the regulated circuit becomes equal to the resistance of the normal circuit is lower than the voltage for a normal cascode circuit. This shows a definite increase in the output swing of the regulated circuit.

In Figure 3.5:

Point 2: V_{omin} (RGC, r) = The minimum output voltage at which the small signal resistances of both circuits become equal.

Point 1: V_{omin} (RGC, s) = The minimum output voltage based on saturation limit. This is the voltage at which T_2 leaves saturation region.

3.3.b DERIVATIONS FOR GAIN

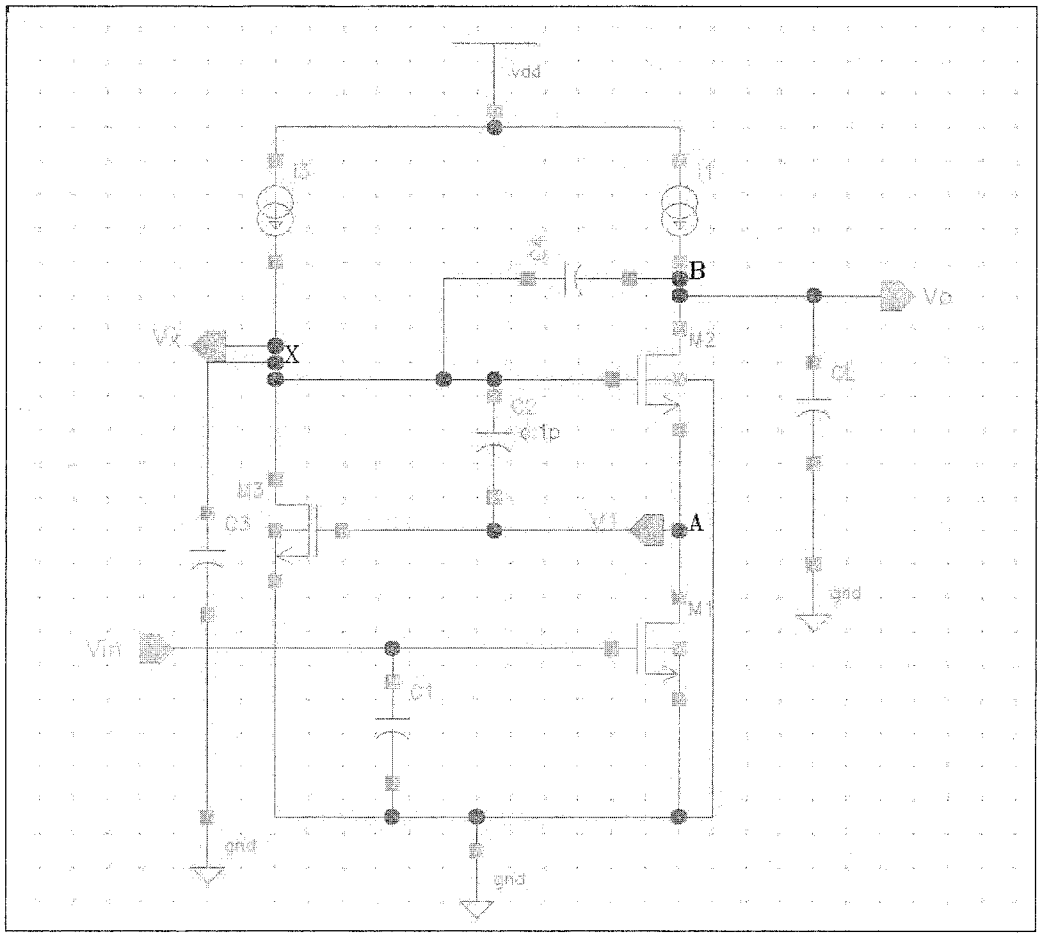


Figure 3.6: Schematic of a basic Gain Boosted Cascode Amplifier

The basic schematic of a gain boosted cascode amplifier is shown in Figure 3.6. M1 and M2 form the main cascode amplifier. Capacitors C1, C2, C3 and C4 are the parasitic capacitances between the different terminals of the transistors. CL is the load capacitance of the amplifier seen at the output node.

The small signal model of this configuration used in the further analysis and derivations is shown in Figure 3.7.

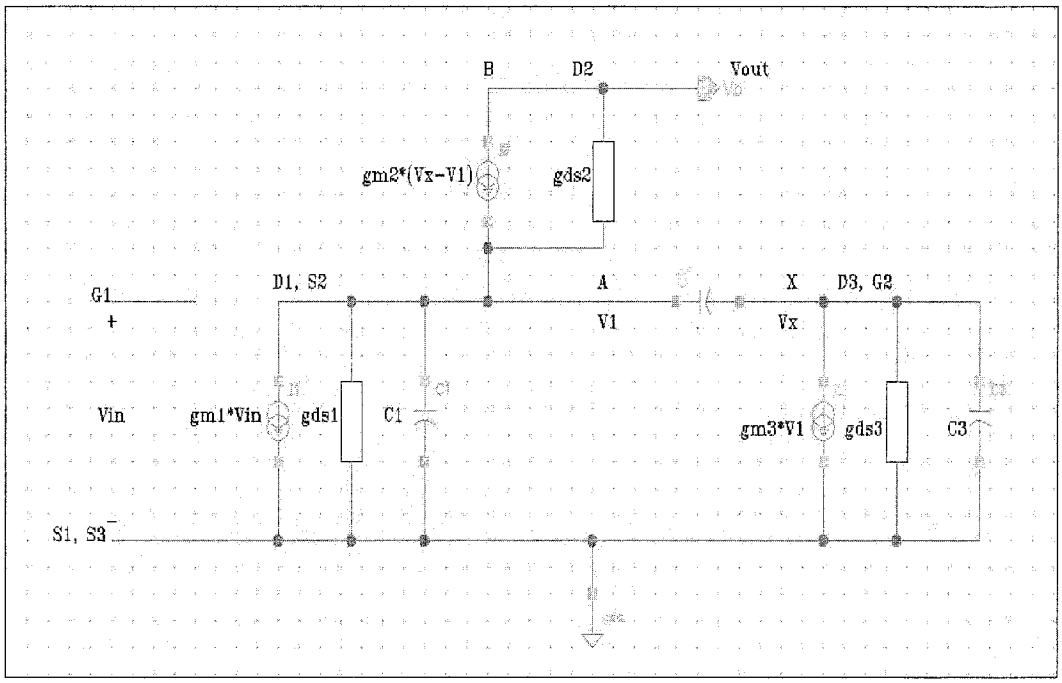


Figure 3.7: Small Signal Model of a basic Gain Boosted Cascode Amplifier

From the small signal model the voltages at the nodes A and X can be given respectively as

$$V_1 = \frac{g_{m1} * V_{in}}{g_{ds1}}$$

$$V_x = \frac{g_{m3} * V_1}{g_{ds3}} = \frac{g_{m3}}{g_{ds1}} * \frac{g_{m1}}{g_{ds1}} * V_{in}$$

Hence the output voltage

$$V_{out} = \frac{g_{m2} * (V_x - V_1)}{g_{ds2}} + \frac{g_{m1} * V_{in}}{g_{ds1}}$$

Substituting for all the voltages in terms of input voltage V_{in}

$$V_{out} = \frac{g_{m2}}{g_{ds2}} \left(\frac{g_{m3} * g_{m1}}{g_{ds3} * g_{ds1}} - \frac{g_{m1}}{g_{ds1}} \right) V_{in} + \frac{g_{m1}}{g_{ds1}} * V_{in}$$

Hence the small signal gain is

$$A_o = \frac{V_{out}}{V_{in}} = \frac{g_{m2}}{g_{ds2}} * \frac{g_{m1}}{g_{ds1}} * \left(\frac{g_{m3}}{g_{ds3}} - 1 \right)$$

Neglecting 1 in comparison to $\frac{g_{m3}}{g_{ds3}}$, we get

$$\therefore A_o \approx \frac{g_{m1} * g_{m2} * g_{m3}}{g_{ds1} * g_{ds2} * g_{ds3}}$$

Substituting $A_3 = \frac{g_{m3}}{g_{ds3}}$, the gain of the feedback amplifier we get

$$A_o = A_3 * \frac{g_{m2} * g_{m1}}{g_{ds2} * g_{ds1}}.$$

Substituting $\frac{1}{g_{ds}} = r_o$, we get

$$A_o = A_3 * g_{m1} * g_{m2} * r_{o1} * r_{o2}$$

This shows that the gain of the regulated (gain boosted) cascode improves by a factor of $A_3 = \frac{g_{m3}}{g_{ds3}}$ over the gain of a normal cascode circuit. This factor is the gain of the feedback amplifier (gain boosting amplifier).

3.3.c STABILITY (POLE-ZERO) ANALYSIS

For the given circuit there are different pole-zero locations as given by the following values:

1) The dominant pole of the whole system at the output of the whole amplifier.

2) Non dominant pole at cascode node (node A):

$$P_A = \frac{g_{m2} * (A_3 + 1)}{C_1 + C_2}$$

3) A pole-zero pair at node X:

A pole due to the 3-dB bandwidth of the boosting amplifier

$$P_X = \frac{g_{ds3}}{C_2 + C_3}$$

A zero due to the feedforward path from the drain of input transistor to the gate of the cascode transistor.

$$Z_X = \frac{g_{m3}}{C_2}$$

The locations of these poles and the corresponding frequency response of a basic gain-boosted cascode amplifier are given in Figures 3.8 and 3.9 below.

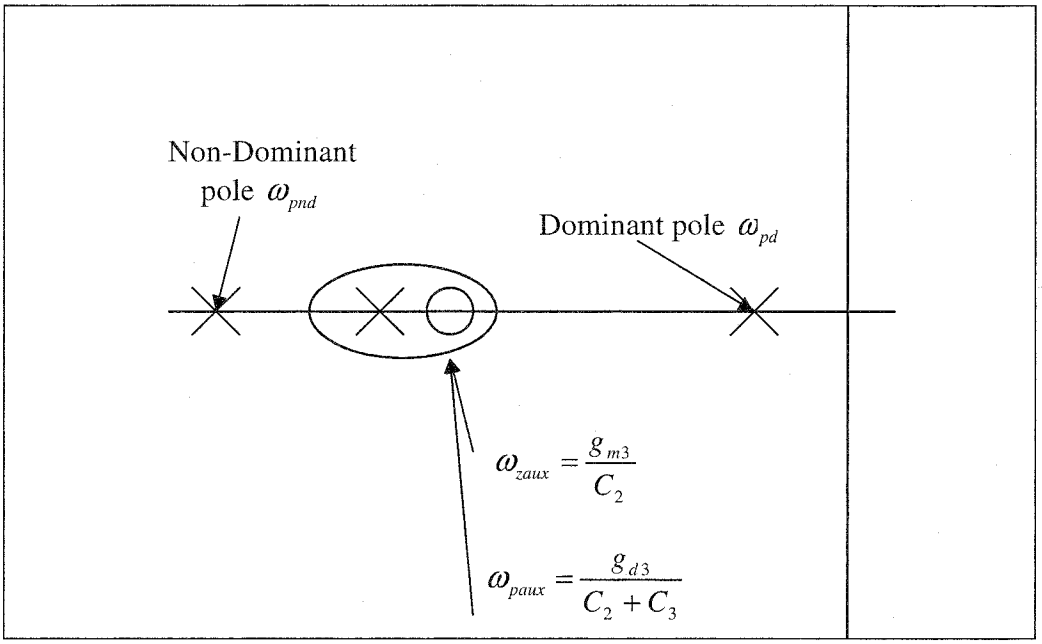


Figure 3.8: Pole Zero locations of a non-optimized gain boosted amplifier.

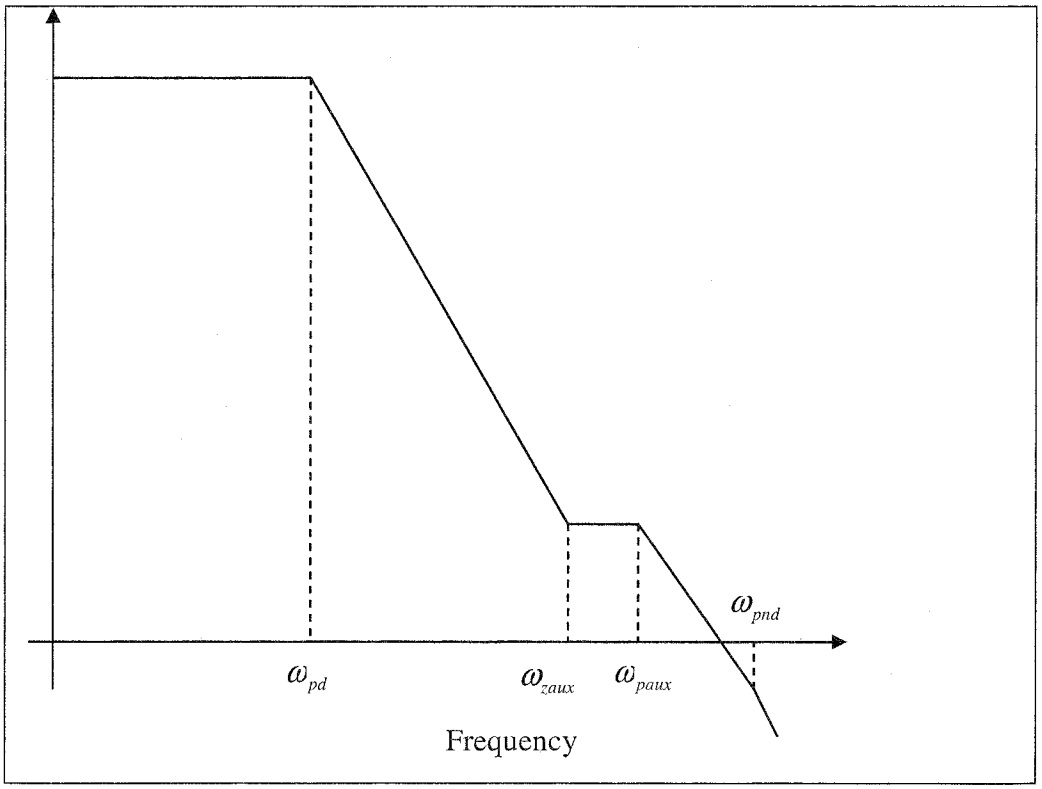


Figure 3.9: Frequency response of a typical gain boosted amplifier

From [18] the transfer function of the Gain Boosted Cascode is given as:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds2}} * \frac{M}{N}$$

where,

$$M = (g_{ds2}C_2 - g_{ds2}C_3 + g_{m2}C_3)S - (g_{ds2}g_{ds3} + g_{m2}g_{m3} - g_{m2}g_{ds3})$$

$$N = (C_1C_3 + C_2C_3 - C_1C_2)S^2 + (g_{m2}C_3 - 2g_{m3}C_2 + g_{ds3}C_1 + g_{m3}C_3 + g_{ds2}C_3 + g_{m2}C_2)S$$

$$+ (g_{m2}g_{ds3} - 2g_{m2}g_{m3} + g_{m3}g_{ds3} + g_{ds2}g_{ds3})$$

The conditions for the optimum compensated gain boosted amplifier will be:

1) The poles P_A and P_X should be complex conjugate poles.

2) The zero Z_X should be beyond the unity gain frequency of the whole amplifier.

Some basic relationships used in the further analysis:

1. $g_{ds} = \lambda * i_{ds}$

2. $g_m = 2 * \frac{i_{ds}}{V_{gst}}$

Using this in the equations for P_X and P_A we get,

$P_X = \frac{\lambda * i_{ds3}}{C_2 + C_3}$ and

$$P_A = \frac{\frac{2i_{ds2}}{V_{gst2}}\left(\frac{2i_{ds3}/V_{gst3}}{\lambda i_{ds3}}+1\right)}{C_1+C_2}$$

For these two poles to be equal, equating $P_X = P_A$

$$\frac{\lambda * i_{ds3}}{C_2+C_3} = \frac{\frac{2i_{ds2}}{V_{gst2}}\left(\frac{2i_{ds3}/V_{gst3}}{\lambda i_{ds3}}+1\right)}{C_1+C_2}$$

$$= \frac{\frac{2i_{ds2}}{V_{gst2}}\left(\frac{2}{\lambda V_{gst3}}+1\right)}{C_1+C_2}$$

$$= \frac{2i_{ds2}}{V_{gst2}}\left(\frac{2+\lambda V_{gst3}}{\lambda V_{gst3}}\right) * \frac{1}{C_1+C_2}$$

$$\therefore i_{ds3} = \frac{2i_{ds2}}{\lambda V_{gst2}} * \left(\frac{2+\lambda V_{gst3}}{\lambda V_{gst3}}\right) * \left(\frac{C_2+C_3}{C_1+C_2}\right)$$

This places a restriction on the amount of small signal current that can flow through the additional gain stage of the system. This is directly related to the speed and bandwidth of the additional gain boosting stage.

3.3.d HIGH FREQUENCY BEHAVIOR

In this section the high frequency behavior of the gain boosted cascode stage is discussed. Figure 3.10 shows the frequency response of the original amplifier (Aorig), the gain boosting stage (Aadd) and the improved stage (Atotal).

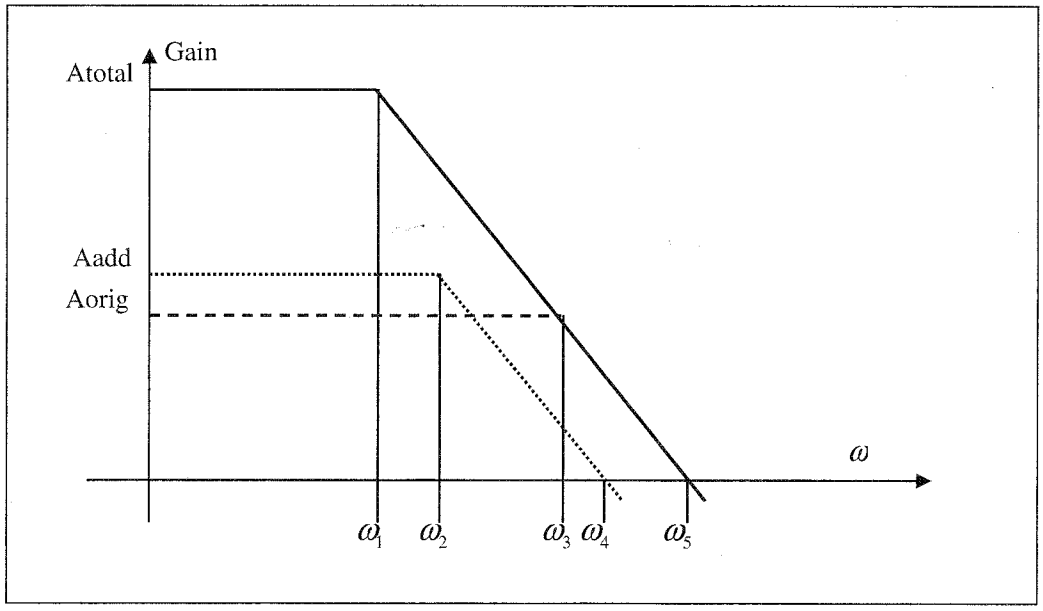


Figure 3.10: Frequency response of the original amplifier (Aorig), the gain boosting stage (Aadd) and the improved stage (Atotal)

In Figure 3.10 at DC the gain enhancement *Atotal/Aorig* will be almost equal to the gain of the additional gain stage. As the frequency increases, first order roll-off occurs. For any frequency $\omega > \omega_1$ the load capacitance results in first order roll-off. Moreover *Aadd* may also have a first order roll-off for $\omega > \omega_2$ as long as $\omega_2 > \omega_1$. This is equivalent to the requirement that the unity gain

frequency of the additional gain boosting stage has to be more than the 3-dB frequency ω_3 of the original stage. But this frequency can be lower than the unity gain frequency of the original stage ω_5. The unity gain frequency of the original and the improved stage are the same.

Hence to obtain a first-order roll-off of the whole system the additional gain boosting stage doesn't have to be an extremely fast stage. In fact, if this stage is very fast then it might cause stability problems due to the closed loop formed with the transistor. This gain boosting stage could be a slow stage with low current levels and non-minimal-length transistors. Considering that the second pole of the main amplifier is at ω_6 (not shown in diagram) a safe range for the location of the unity gain frequency of the additional stage is taken to be $\omega_3 < \omega_4 < \omega_6$.

3.3.e SETTLING BEHAVIOR

As shown in Section 3.3.c the addition of gain boosting amplifiers adds a pole-zero doublet in the system. A pole-zero doublet introduces a slow settling component and slows down the settling behavior of the system. Incomplete doublet cancellation can seriously degrade the settling behavior of the amplifier [19]. So one solution is to make this slow settling component fast enough so as not to affect the settling time of the amplifier. This can be achieved when the unity gain frequency of the additional stage is higher than the -3 dB frequency of the complete system. The settling behavior depends on the locations of the pole-zero doublet in the system. So the thing to be considered is to push this doublet beyond the unity gain frequency of the system. This will get rid of the slow settling component thereby not affecting the settling time of the amplifier. These factors can be taken care during the designing of the amplifier and additional gain stages.

Chapter 4

A DESIGN CASE: GAIN BOOSTED TELESCOPIC CASCODE AMPLIFIER

This chapter presents a design of a gain boosted telescopic cascode amplifier. This design is presented as a proof of concept for the previously mentioned gain boosting technique. An operational amplifier with open loop gain A_o > 85 dB and unity gain frequency > 80 MHz is designed using RIT's 2 μm technology.

4. 1 DESIGN SPECIFICATIONS

Based on some of the previously described work in the literature review (Section 2.2), the amplifier to be designed has the following requirements:

1. Open Loop Gain $A_o > 85$ dB
2. Unity Gain Frequency > 80 MHz
3. Phase Margin > 55 degrees
4. Load Capacitance: 1 pF
5. VDD = 5 V, VSS = 0
6. Input Common Mode Range ICMR: 1.5 V – 3.5 V
7. Output Common Mode Range: 1.5 V – 3.5 V
8. Output Swing: 1.5 V – 3.5 V
9. Power Dissipation < 10 mW

A telescopic OTA was used because of its simplicity over other designs, allowing for higher-speed operation. Based on the results of Table 2.1, a telescopic cascode gives medium gain with highest speeds. Introducing gain boosting into the telescopic cascode should lead us to high gain and at the same time not affect the speed a lot. This leads to the use of telescopic cascode architecture in this design.

Also, in a folded-cascode design, there is an input differential pair and two separate current branches for the differential output. The input currents are mirrored with a cascoded configuration to produce the output currents. The telescopic architecture puts both the input differential pair and the output on the same two current branches. This approach eliminates the noise problems caused by the current mirrors and also leads to a more direct signal path, which allows for higher speed. Another advantage of the telescopic architecture is that it uses half the bias current of a folded-cascode design because it has two fewer branches for current.

In this section the implementations of the main op-amp and the additional gain stages are discussed. The main stage used is the telescopic cascode differential amplifier. The simplest implementation of the additional gain stages used in this design is a single transistor common source amplifier.

4. 2 TELESCOPIC OTA ARCHITECTURE

The telescopic OTA used as a final design is shown in Figure 4.1.

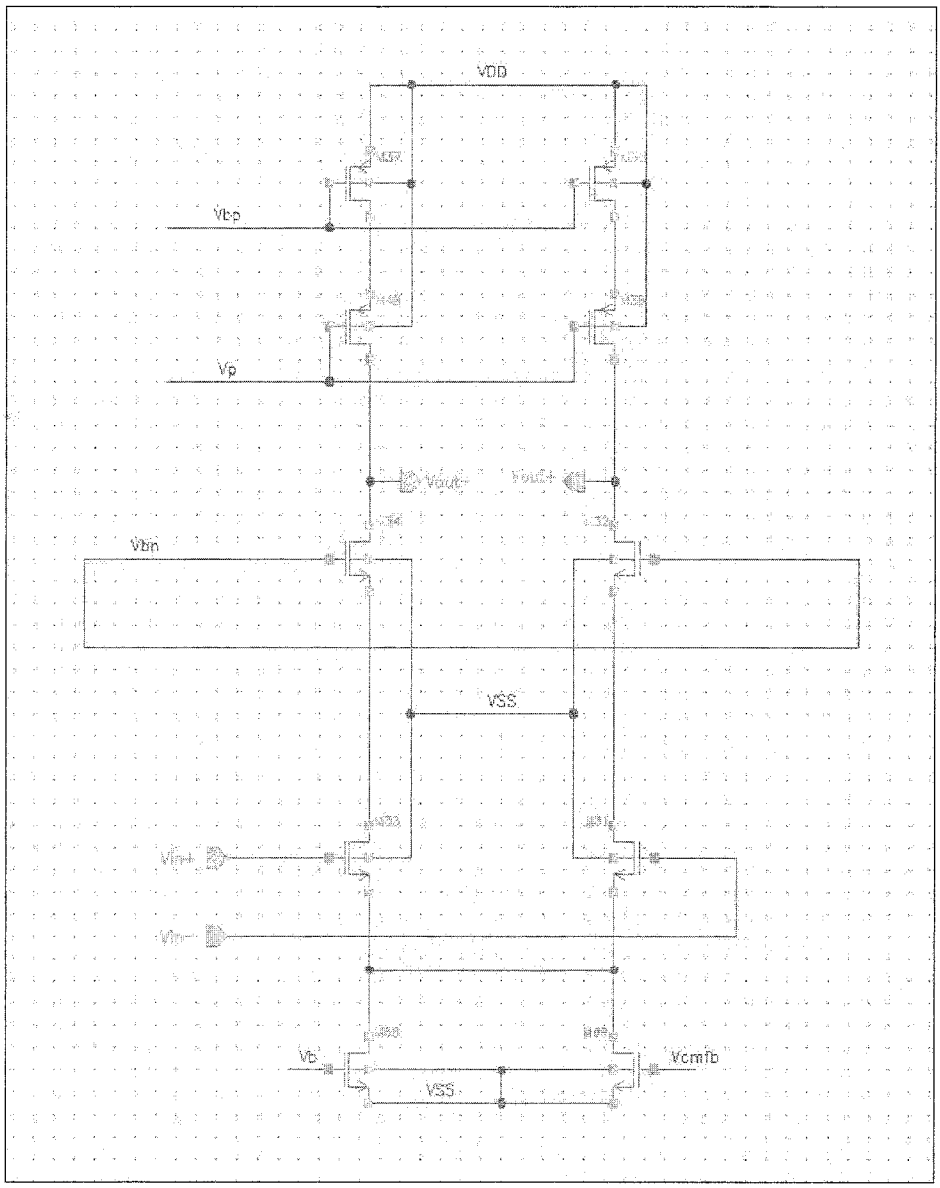


Figure 4.1: A fully differential telescopic cascode architecture

A differential pair M33 and M31 is used to sense the input voltage difference. If the pair is operating in saturation, when one transistor is turned on, the other will turn off. The current through one leg will be sourced to the output while the other leg will sink current from the load.

Special care must be taken to ensure that the input differential pair (M33 and M31) is operating in saturation and not in the triode region. Operation in the triode region will cause the behavior of the OTA to be nonlinear and will result in poor transient response as well as a loss in DC gain.

The telescopic architecture differs from other approaches because the common mode of the input is different from the common mode of the output for the input differential pair to be in saturation and operate linearly. This will have to be taken into consideration before the telescopic design is used in a larger circuit. If the outputs are to be used as inputs to another OTA, their common mode must first be adjusted using a common mode feedback circuit. This circuit is described later in the chapter.

4. 3 Gain-Boosting

The idea of gain-boosting is shown in Figure 4.2.

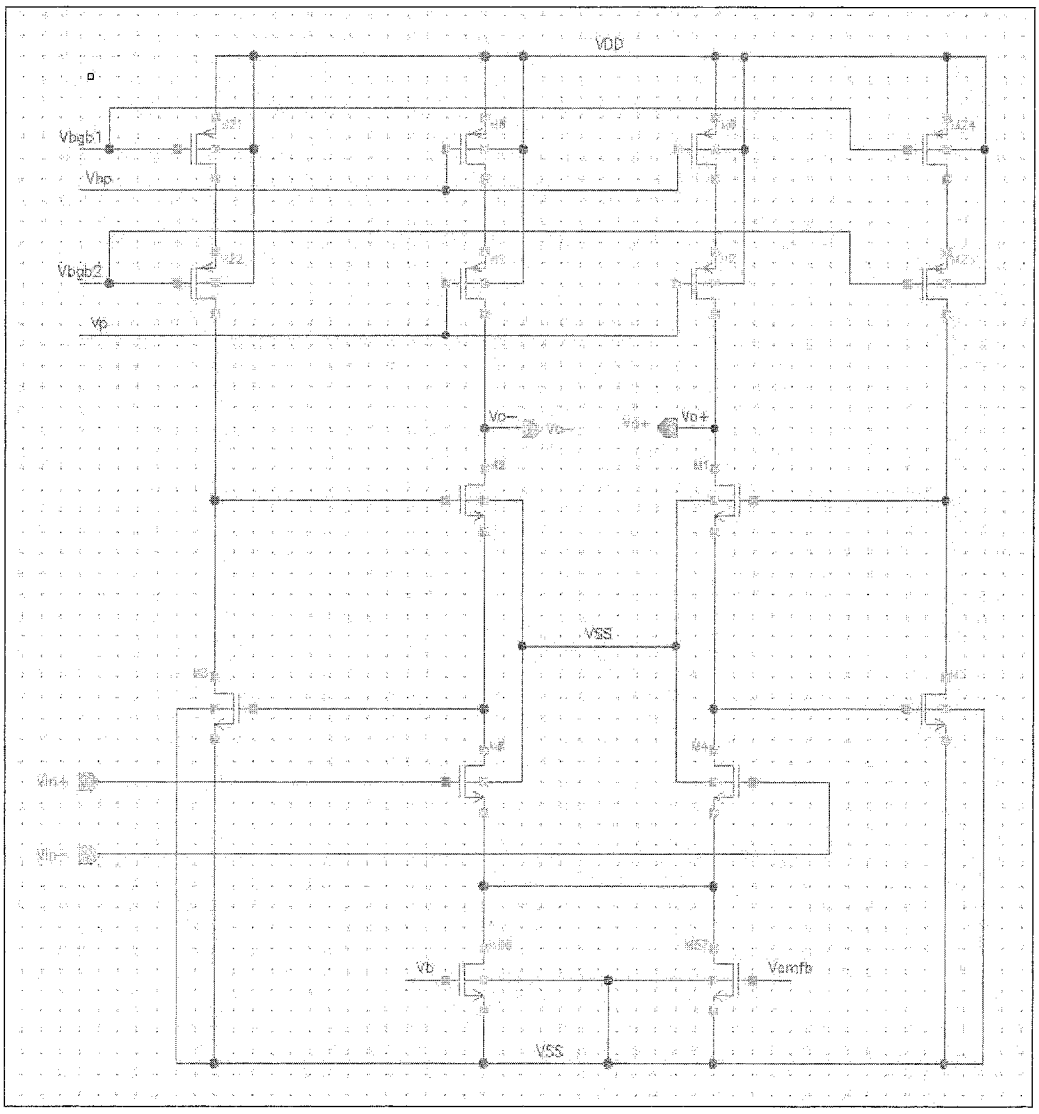


Figure 4.2: A fully differential telescopic cascode with gain boosting architecture

Essentially transistors M3 and M5 are acting as simple common-source NMOS amplifiers with cascode current loads. The output of these auxiliary

amplifiers is providing an output voltage to bias the gates of M2 and M1. The gain of this auxiliary amplifier is multiplied by the gain of the telescopic section to provide a much higher DC gain. The result is better settling accuracy without affecting the speed of the circuit, since it does not add gates into the signal path.

There has been research done to show that gain-boosting also improves settling time [8], [18], [20]. Increasing the current through the auxiliary amplifiers moves the non-dominant poles of the circuit to the imaginary axis as shown earlier. This also has the effect of increasing the unity gain bandwidth of the circuit. At some point, the gain of the auxiliary amplifiers is reduced to the point where the circuit does not settle to the desired accuracy. As is shown in Chapter 3, too much increase in current might also lead to instability because high currents in the additional stage will give high unity gain frequency for the additional stage and the relationship given in Sections 3.3.d and 3.3.e will not be maintained.

4. 4 Wide-Swing Cascode Bias Network

The biasing network shown in Figure 4.3 is based on the popular Wilson current mirrors (wide-swing cascode current mirrors). Cascode sources were chosen because it was necessary to keep the bias currents in the top half of the telescopic amplifier as constant as possible to ensure accurate settling. One transistor in the cascode configuration mirrors the current while the other basically acts as a buffer between the current source and changing voltages in the circuit. The wide-swing configuration reduces signal swing limitations encountered with normal cascode biasing.

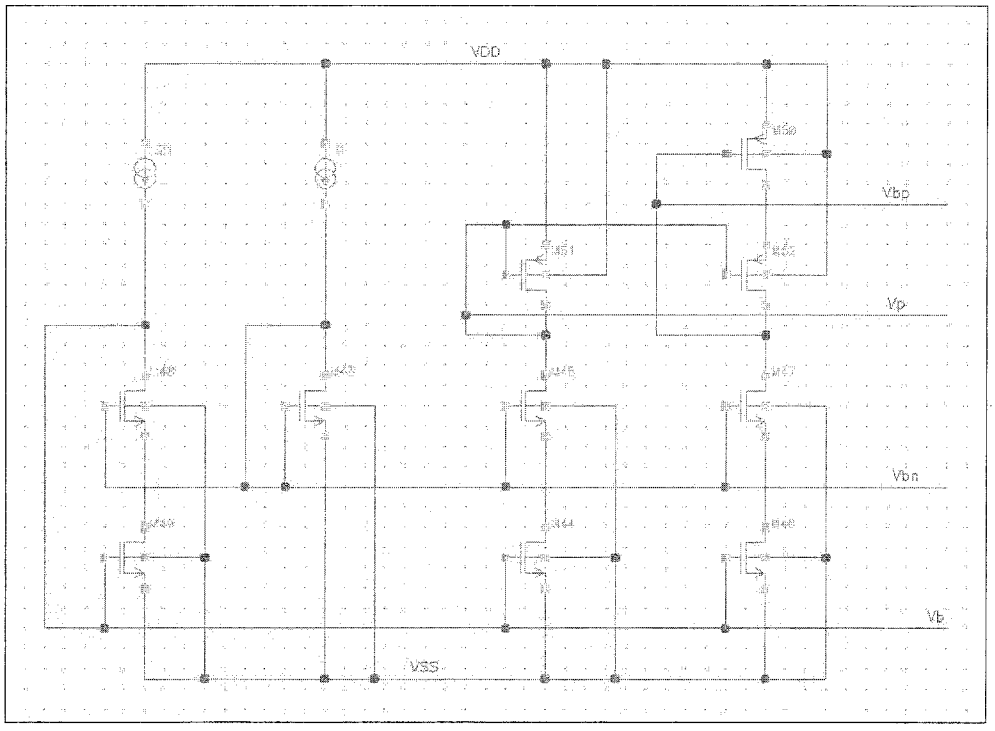


Figure 4.3: A Wide Swing Cascode Biasing circuit

4. 5 Common-Mode Feedback

Common-mode feedback is necessary in a fully differential OTA to keep the outputs from drifting high or low out of the range where the amplifier provides plenty of gain.

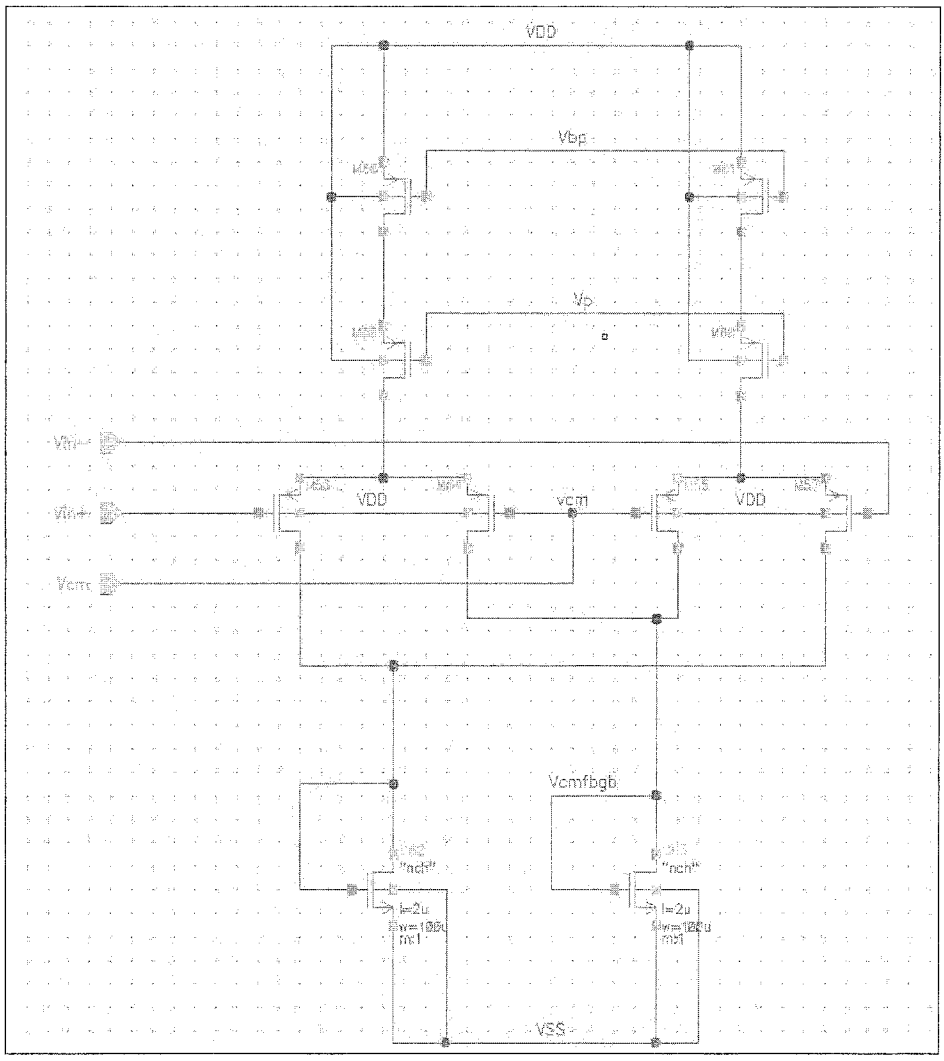


Figure 4.4: Common Mode feedback circuit.

This circuit uses two differential pairs (M53, M54 and M55, M57) to sense the difference between the average output voltage and a common mode voltage *Vcm* which is supplied externally. *Vcmfgb* is used to bias a transistor that adds to the bias current and keeps the common mode from drifting up. The current in the CMFB circuit does not need to be large as long as the currents through the top and bottom of the OTA are fairly well balanced. Since the common-mode feedback circuit only adds to the bias current in the bottom of the circuit, it is expected that the bias currents in the top half will be slightly lower.

4. 6 DESIGN PROCEDURE

The design procedure is divided into two steps. First step is to design the normal telescopic cascode and the second step is to insert the gain boosting amplifiers to obtain the desired gain from the configuration without affecting the bandwidth to a large extent.

The telescopic cascode design starts with the sizing of the main differential input pair of transistors M0 and M4 using the desired phase margin and gain bandwidth specifications. As these are the two factors that affect the input pair transistors they are first designed to meet the required specifications. Care has to be taken not to make the input pair too big to affect the bandwidth and at the same time making them big enough to provide enough transconductance and hence the gain.

The NMOS M1 and M2 cascode transistors are then sized to act as a buffer between the input pair and the output. These transistors are sized such as not to load the output nodes with huge parasitic capacitances so as to affect the bandwidth of the amplifier.

The PMOS cascode load transistors are designed to steer the required amount of current through both the legs. Here again the PMOS cascode transistors are sized so as not to load the output with huge parasitic capacitances.

With the basic design the gain of the amplifier was found to be 70 dB. This was much less than the required gain of 85 dB. So gain boosting amplifiers were inserted into the circuit to increase the gain up to the required values.

The overall gain is in general increased by approximately the gain of the gain-boost amplifiers; the gain specifications of the gain-boost amplifiers were thereby known. The unity gain frequency of the gain-boost amplifiers should be large enough so that they do not significantly affect the frequency behaviour of the overall amplifier. They will reduce the unity gain frequency of the overall amplifier since by adding the gain-boost amplifiers to the output side, extra capacitance and thereby some extra poles are added.

The bias current should be as low as possible, still allowing high enough unity gain frequency. Since the gain only had to be increased by about 15 dB, a NMOS common source amplifier biased with a cascode current source was chosen as gain-boost amplifier. It should give high enough gain and it is not very complex, it should thereby be easy to get sufficiently high unity gain frequency and it should not degrade the performance of the overall amplifier too much.

The simulation and sweeping of parameters were performed. When they were working according to the demands, they were connected to the main amplifier and the performance of the overall amplifier was verified.

The gain had increased, but both the unity gain frequency as well as the phase margin was degraded too much. The bias currents of the main amplifier were then increased and some of the bias voltages were altered. Since the output DC-level of the gain boost amplifiers can be chosen from a wider range than the bias voltages, this was another benefit of using gain boosting. In a way they give both increased gain and voltage level shift although at the cost of added complexity, additional layout area and higher power consumption.

After several iterations, an amplifier that fulfilled all the demands on the performance was found.

4. 7 RESULTS and PLOTS

TRANSIENT RESPONSE:

The transient response of the amplifier is shown in Figure 4.5. The transient response was taken for a sinusoidal input of low amplitude so as to not to saturate the amplifier. The plot shows the outputs of the OTA for a sine wave input. This plot shows that the common mode of the output voltage settles to the desired level that is set by the common mode feedback circuit (in this case it is set to half the supply voltage).

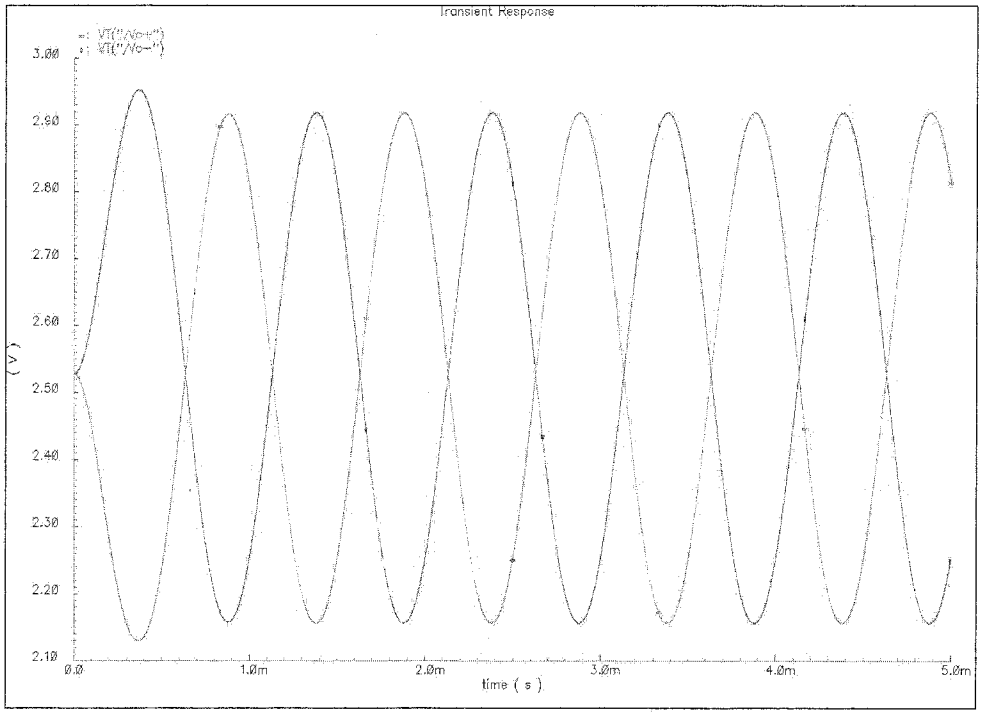


Figure 4.5: Transient Response of the Telescopic Cascode OTA

AC RESPONSE:

The AC response of the designed amplifier is shown in Figure 4.6. This plot gives us the values of DC gain, the frequency response of the amplifier and the phase margin values. The open loop DC gain of the OTA is found to be 92 dB. The unity gain frequency of the amplifier is 88 MHz. The phase margin obtained at this point is 63 deg.

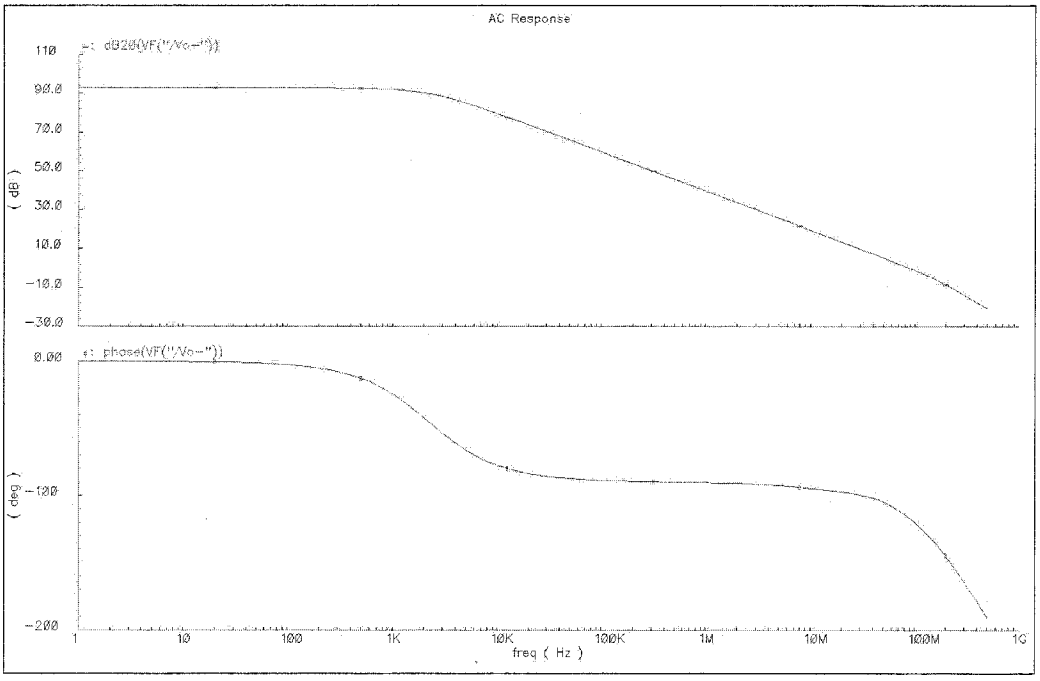


Figure 4.6: AC Response of the Telescopic Cascode OTA

INPUT COMMON MODE RANGE (ICMR):

The plot in Figure 4.7 shows the effect of variation in the input common mode voltage on the output common mode level. This test was done for the output common mode level at 2.5 V. The figure shows that for the input common mode voltage of 1.6V and higher the output common mode voltage (DC level) stays at the desired level. The gives the input common mode range of the circuit. This range is 1.6V – 3.5V.

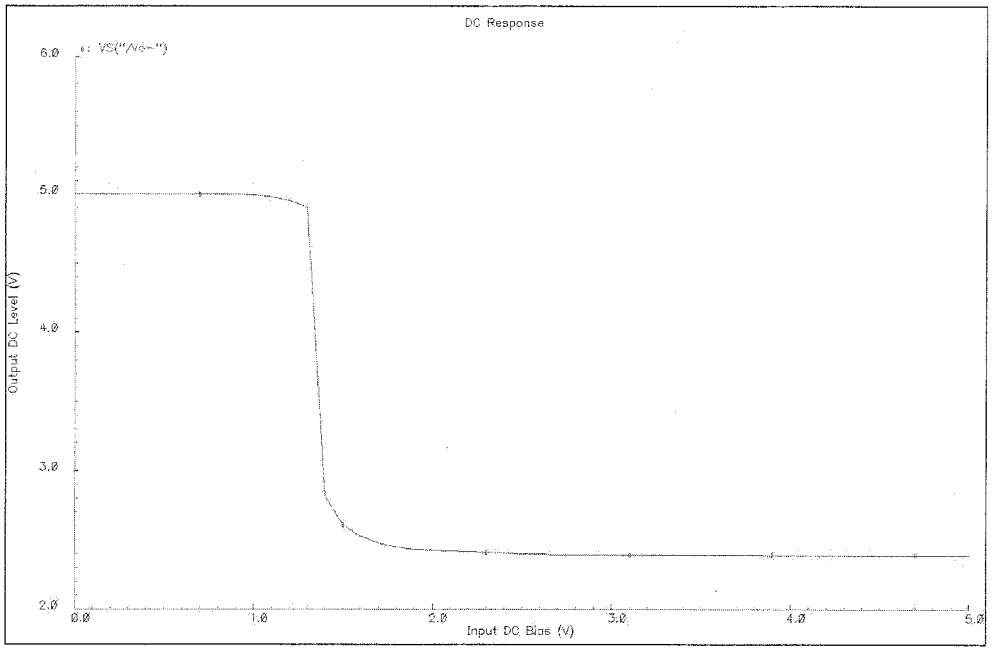


Figure 4.7: Effect of variation input common mode voltage.

SLEW RATE MEASUREMENT:

The slew rate is calculated by changing the inputs of the OTA to square wave inputs with 5 V amplitude, and measuring the slope at the differential output of the OTA. The plot in Figure 4.8 shows the input step response of the designed OTA. The slope of the output gives the slew rate of the amplifier. The slew rate of the designed amplifier is 65 V/µsec. Various techniques which use special circuits are available to boost this slew rate of the circuit.

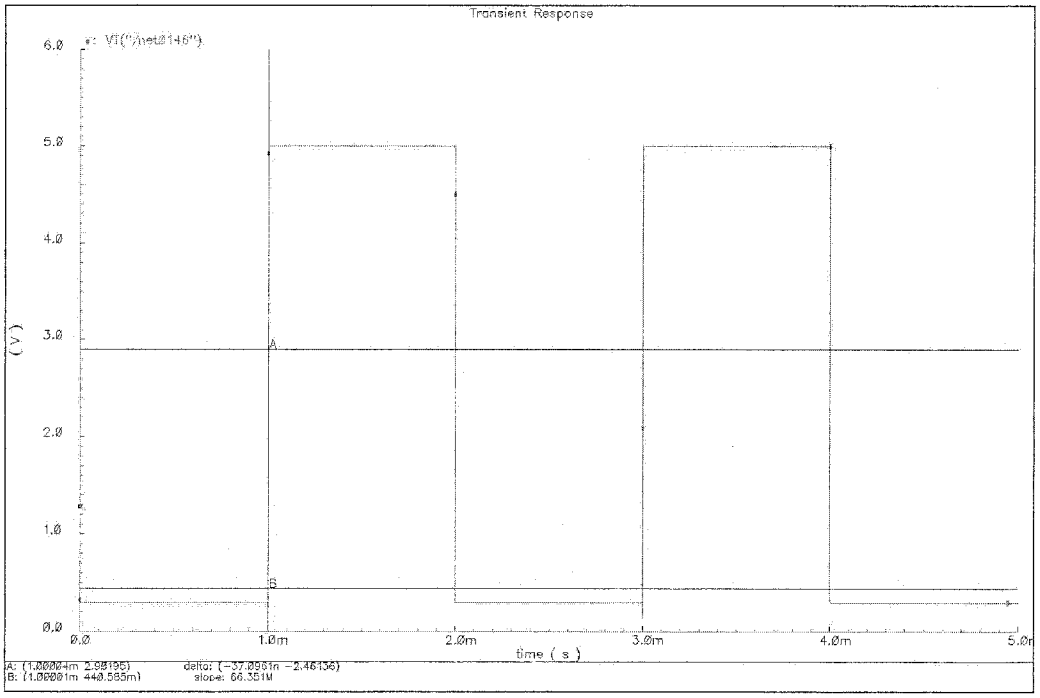


Figure 4.8: Slew Rate measurement of the Telescopic Cascode OTA

COMMON MODE FEEDBACK CIRCUIT USABLE RANGE:

The plot in the Figure 4.9 shows the voltage range of the common mode Feedback Circuit. This is the range for which the output common mode voltage follows the input common mode voltage which is one of the inputs to the CMFB circuit and is set externally. This range places a limit on the output common mode range of the amplifier. For the designed circuit this range is found to be 0.6 V – 3.3 V. Although the CMFB circuit works well for voltage as low as 0.6 V, but this value of common mode voltage kills the gain of the circuit as it pushes the input transistors out of saturation. Based on gain variation the usablity range is limited to 1.6 V to 3.3 V.

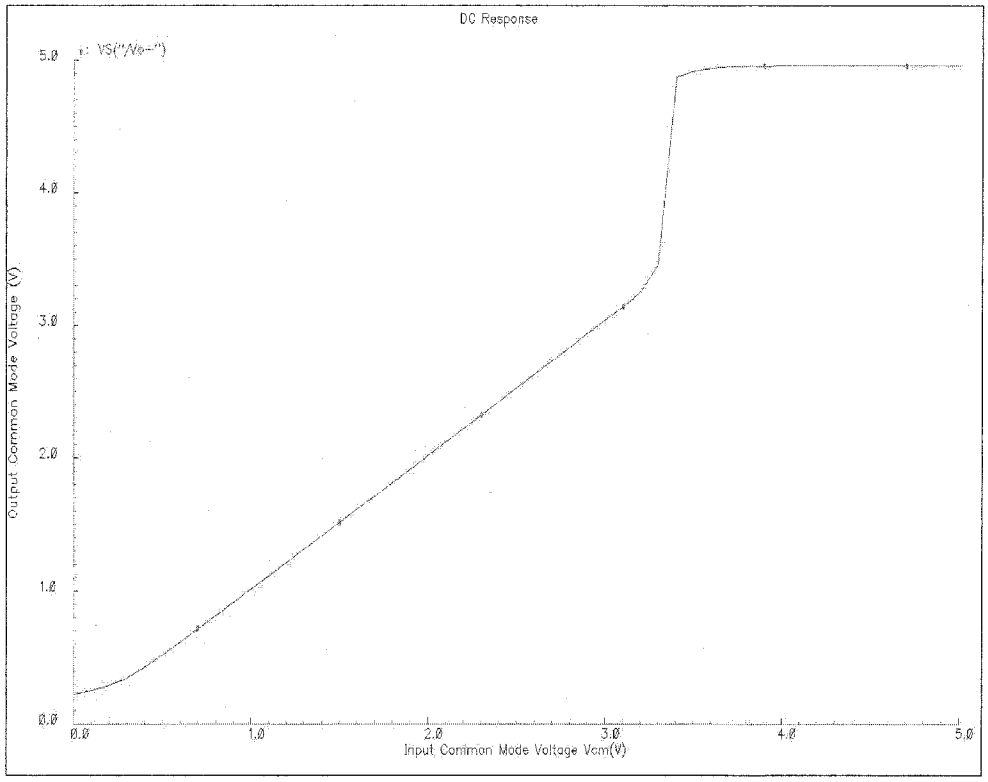


Figure 4.9: Common Mode feedback circuit usability range.

4. 8 FINAL SIMULATION RESULTS

Parameter	Value
DC Gain without gain boosting	73 dB
DC Gain with gain boosting	92 dB
Unity Gain Bandwidth	88 MHz
Phase Margin	63 deg
Slew Rate	65 MV/sec
ICMR	1.5 V – 3.6 V
OCMR	1.6 V - 3.2 V
Output Swing	1.8 V – 3.5 V
PSRR (Change in Gain for $\pm$ 10 %VDD)	7.8 dB
Power dissipation	9 mW

Chapter 5

CONCLUSION AND FUTURE WORK

5.1: Conclusion

5.2: Future Work

CONCLUSION

The goal of this work was to design a high gain operational amplifier. An OTA with 92 dB gain and 88 MHz unity gain frequency has been successfully designed using RIT's 2 μm process. In this work effort is made to understand various topologies of the existing operational amplifier being used to meet high gain requirements, identify the limitations of these circuits, and then overcome these limitations.

The architecture used in this work uses gain boosting techniques to increase the gain of the amplifier. Applying this architecture to a telescopic cascode configuration, an operational amplifier with a gain of 92 dB and a unity gain frequency of 88 MHz has been designed.

FUTURE WORK

In this work a gain boosting technique has been applied to telescopic cascode configurations. This could also be applied to a conventional two stage amplifer or a folded cascode configuration.

The unity gain bandwidth of the circuit is still not very high. Using the present sub-micron technologies, very high bandwidths could be realized. Some work can be done to improve this aspect of the design. Also, the slew rate could be increased by the use of special slew rate boosting circuits. It should be possible to scale this design down to the present day technologies without making large scale modifications. Scaling might need some minor recalculations.

The amplifer presented in this work does not use an output stage. An output stage can be added to the design which will not only increase the gain further but at the same time might lead to higher output swing. Using various fancier output stages, it could be possible to obtain a high swing amplifer with high gain and high bandwidth at the same time. However, this will require the use of proper compensation techniques which will increase the complexity of the circuit.

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